PhD in Information Technology and Electrical Engineering
Università degli Studi di Napoli Federico II

PhD Student: Vincenzo Terracciano

Cycle: XXXVIII

Training and Research Activities Report

Year: First

Tutor: prof. Andrea Irace

Co-Tutor: prof. Vincenzo d'Alessandro

Date: October 18, 2023

Training and Research Activities Report

PhD in Information Technology and Electrical Engineering

Cycle: **Author:**

1. Information:

- **PhD student: Vincenzo Terracciano**
- **DR number: DR996633**
- **Date of birth: 23/03/1993**
- **Master Science degree: Electronic Engineering University: Federico II**
- **Doctoral Cycle:XXXVIII**
- **Scholarship type: DIETI**
- **Tutor: Andrea Irace**
- **Co-Tutor: Vincenzo d'Alessandro**

2. Study and training activities:

Activity	Type[1]	Hours	Credits	Dates	Organizer	Certificate[2]
Quantum Complexity	seminar	1	0.2	10/11/2022	Prof. Alioscia Hamma	N
SSM Scientific Colloquia	seminar	1	0.2	17/11/2022	Prof. Pietro De Lellis	N
2023-Industry 4.0 Fundamentals in Bosch Applications	seminar	10	2	23-26/01/2023	Eng. Martino Bruni	Y
How to boost your PhD	course	16	4	11-18-25/01 - 1-8-15-22/02 - 1/03/2023	Dr. Antigone Marino	Y
The Hours of the Sun. Astronomy, Geometry, and Art in Ancient Sundials	seminar	1	0.2	18/05/2023	Prof. Alessandra Pagliano	N
Teoresi gruop	seminar	2	0.4	26/05/2023	Prof. Giuseppe Ruello	N
Cylindrical Micro- and Nanowires: From Curvature Effects on Magnetization to Sensing Applications	seminar	1	0.2	20/06/2023	Prof. Manuel Vázquez	N
Modeling Clustered Seismicity Risk: Are We Ready?	seminar	1	0.2	22/06/2023	Prof. Paolo Bazzurro	N
Traffic Engineering with Segmented Routing: optimally addressing popular use cases	seminar	1	0.2	23/06/2023	Prof. Pascal Merindol	N

Fulbrighters Fredericiani a Ingegneria	**seminar**	**2**	**0.4**	**26/06/2023**	**Prof. Giuseppe Ruello Prof. Riccardo Lattanzi**	**N**
Insights into the Design of Transmit and Receive Coils for Ultra-High Field MRI	**seminar**	**2**	**0.4**	**29/06/2023**	**Prof. Riccardo Lattanzi**	**N**
BGP & Hot-Potato Routing: graceful and optimal convergence in case of IGP events	**seminar**	**1**	**0.2**	**30/06/2023**	**Prof. Pascal Merindol**	**N**
Optimization of a mobile clinic routing and scheduling problem in equitable vaccination outreach	**seminar**	**1**	**0.2**	**21/06/2023**	**Prof.Mingyao Qi**	**N**
Academic Entreprenuership	**course**	**12**	**4**	**29-31/05 05-15-20-22/06/2023**	**Prof. Pierluigi Rippa**	**Y**
CI-LAM 2023	**Doctoral School**	**37.5**	**4**	**17-21/07/2023**	**Prof. Giovanni Breglio**	**Y**
Electrodynamics of Continuous Media	**course**	**70**	**9**	**March-June 2023**	**Prof. Claudio serpico**	**Y**
Introduction to Formal Verification of Digital Design and Jasper Apps	**seminar**	**2**	**0.4**	**18/10/2023**	**Ing.Massimo Roselli (Company: Cadence)**	**N**

1) Courses, Seminar, Doctoral School, Research, Tutorship
2) Choose: Y or N

2.1. Study and training activities - credits earned

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	**0**	**0.4**	**9.6**	**0**	**10**
Bimonth 2	**0**	**2**	**8**	**0**	**10**
Bimonth 3	**4**	**0**	**6**	**0**	**10**
Bimonth 4	**0**	**2.4**	**7.6**	**0**	**10**
Bimonth 5	**4**	**0**	**6**	**0**	**10**
Bimonth 6	**13**	**0.4**	**0**	**0**	**13.4**
Total	**21**	**5.2**	**37.2**	**0**	**63.4**
Expected	**30 - 70**	**10 - 30**	**80 - 140**	**0 – 4.8**	

3. Research activity:

Power electronics technologies provide electrical energy conversion, primarily using solid-state semiconductor devices and passive components. The global power device market reaches US$40 billion (https://www.imarcgroup.com/power-semiconductor-market) and is rapidly expanding, driven by emerging applications such as electric vehicles, data centres, electric grids, and renewable energy processing. In power electronics systems, power devices are used as solid-state switches. Ideal power devices should be able to conduct infinite current with minimal resistance, block infinite voltage and switch at infinite frequency with zero power loss. Translated to practical devices, these conditions correspond to low on-state resistance (R_{ON}), high breakdown voltage (BV), and small switching losses. The trade-offs between these device metrics usually determine the efficiency, frequency, and power density of an entire power electronics system. Thus, innovation in power device engineering is a key driver for energy savings and associated reductions in carbon dioxide emissions. There are two main approaches to improve these trade-offs in power devices: (*i*) The first approach is to employ semiconductors with superior properties for power switching, such as wide-bandgap (WBG) materials, while (*ii*) the second approach involves innovation in device architecture.

My research work focuses on the above approaches. More specifically, I have been involved in improving the architecture of power semiconductor devices in silicon carbide (SiC) technology. In the work *"SiC GAA MOSFET Concept for High Power Electronics Performance Evaluation through Advanced TCAD Simulations"*, a groundbreaking SiC power MOSFET based on innovative vertical Gate All Around (GAA) concept is presented, where through a massive campaign of TCAD (Technology Computer Aided Design) simulations, it was possible to observe a decrease in R_{ON} compared to the usual planar MOSFETs, while maintaining a relatively high BV.

Another part of my work is to develop a SPICE-compatible model for describing the static behavior of a particular class of SiC diodes denoted as Merged PiN Schottky (MPS), also considering the *snapback* which is a particular mechanism that can lead to *current focusing* as multiple MPS devices are connected in parallel. This SPICE-compatible model, presented in the work titled "*A Geometry-Scalable Physically-Based SPICE Compact Model for SiC MPS Diodes Including the Snapback Mechanism*" can be particularly useful and convenient in evaluating and preventing the impact of snapback to ensure safe parallelization of multiple devices. Moreover, thanks to this compact model, it is possible to estimate with good accuracy the behavior of SiC MPS cells in conditions not feasible for TCAD analysis, such as converter-level simulations. In

addition, the model can also account for electrothermal effects, and the consequent current capability degradation can be quantified, as described in the work titled *"A Simple Electrothermal Compact Model for SiC MPS Diodes Including the Snapback Mechanism"*. Therefore, the presented models can be a valuable support for both the design and optimization of SiC MPS cells and for an estimation of the impact of snapback, drastically reducing the complexity and time required by a standard TCAD simulation.

4. Research products:

V. d'Alessandro, **V. Terracciano**, A. Borghese, M. Boccarossa, and A. Irace *"A Simple Electrothermal Compact Model for SiC MPS Diodes Including the Snapback Mechanism"*, 29th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), 2023.

V. Terracciano, A. Borghese, M. Boccarossa, V. d'Alessandro, and Andrea Irace "*A Geometry-Scalable Physically-Based SPICE Compact Model for SiC MPS Diodes Including the Snapback Mechanism"*, International Conference on Silicon Carbide and Related Materials (ICSCRM), 2023.

L. Maresca, **V. Terracciano**, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, A. Mihaila, G. Romano, S. Wirths, L. Knoll, and A. Irace *"SiC GAA MOSFET Concept for High Power Electronics Performance Evaluation through Advanced TCAD Simulations"*, International Conference on Silicon Carbide and Related Materials (ICSCRM), 2023.

5. Conferences and seminars attended

• *China-Italy Joint Laboratory on Advanced Manufacturing (CI-LAM 2023), Napoli, Italy, 17- 21 July 2023.* **Doctoral School**.

• *International Conference on Silicon Carbide and Related Materials (ICSCRM), Sorrento, Italy, 17-22 September 2023.* **Poster presentation**.

• *29th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), 27-29 September 2023.* **Oral presentation**.