



UNIVERSITÀ DEGLI STUDI DI NAPOLI  
FEDERICO II

itee<sup>PhD</sup>  
information technology  
electrical engineering



# Manuel Maddaluno

## Workload-driven High-Performance Reconfigurable Architectures

Tutor: Prof. Alessandro Cilardo

Cycle: XXXIX

Year: Second

# Candidate's information

- **MSc degree:** Computer Engineering
- **DIETI Research group/laboratory:** SECLAB
- **PhD start date:** 29<sup>th</sup> December 2023
- **Scholarship type:** PNRR – Centro Nazionale CN1 - National Centre for High-Performance Computing, Big Data and Quantum Computing – Spoke: Future HPC

# Summary of study activities

- **Ad Hoc PhD Courses:**

- How to boost your PhD
- Innovation and Entrepreneurship
- High-Performance and Quantum Computing

- **Seminars:**

- Solid State Transformers: Fundamentals, Insights and New Trends
- Can we Rely on AI? Reliability Issues in Artificial Neural Networks and Potential Solutions for Autonomous Vehicles
- The Good, the Bad, and the Ugly in Quantum Computing: Computational Power, Intrinsic Noise, and Transient Faults
- Dynamic Risk Assessment: Industrial Applications Leveraging Bayesian Inference for Enhanced Decision Making
- 5G & Digital Transformation: A View From An Unconventional Perspective
- PhD Survival Strategies
- Sovranità digitale cos'è e quali sono le principali minacce al cyberspazio nazionale
- Superconducting Radio Frequency Cavities for Quantum Computing and Communication
- Trusted Execution Environments for QPUs
- Guardians Of Threats? AI at the Frontlines of Cybersecurity

# Research field

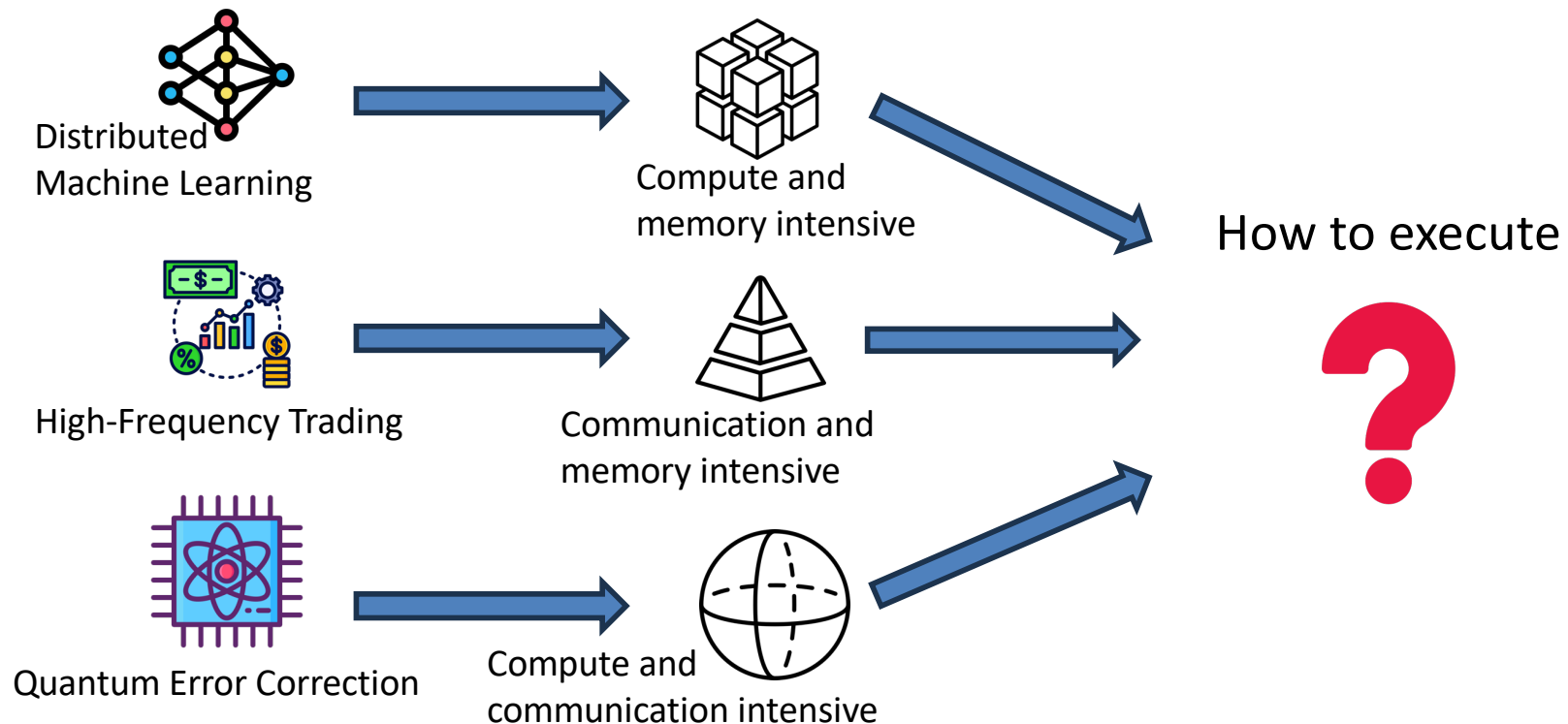
- The main topic of my research is **High-Performance Computing (HPC) architectures**.
- During my second year I investigated how to **adapt the architecture** based on the **workload**.



# Research Activity

- **Problem**

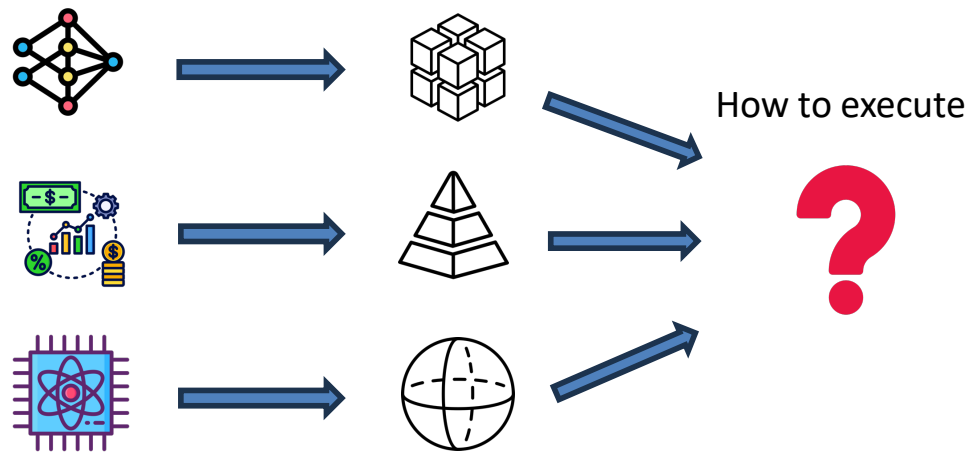
- **Different applications** have different requirements and generate **different types of workload**



# Research Activity

- **Problem**

- Different applications have different requirements and generate **different types of workload**

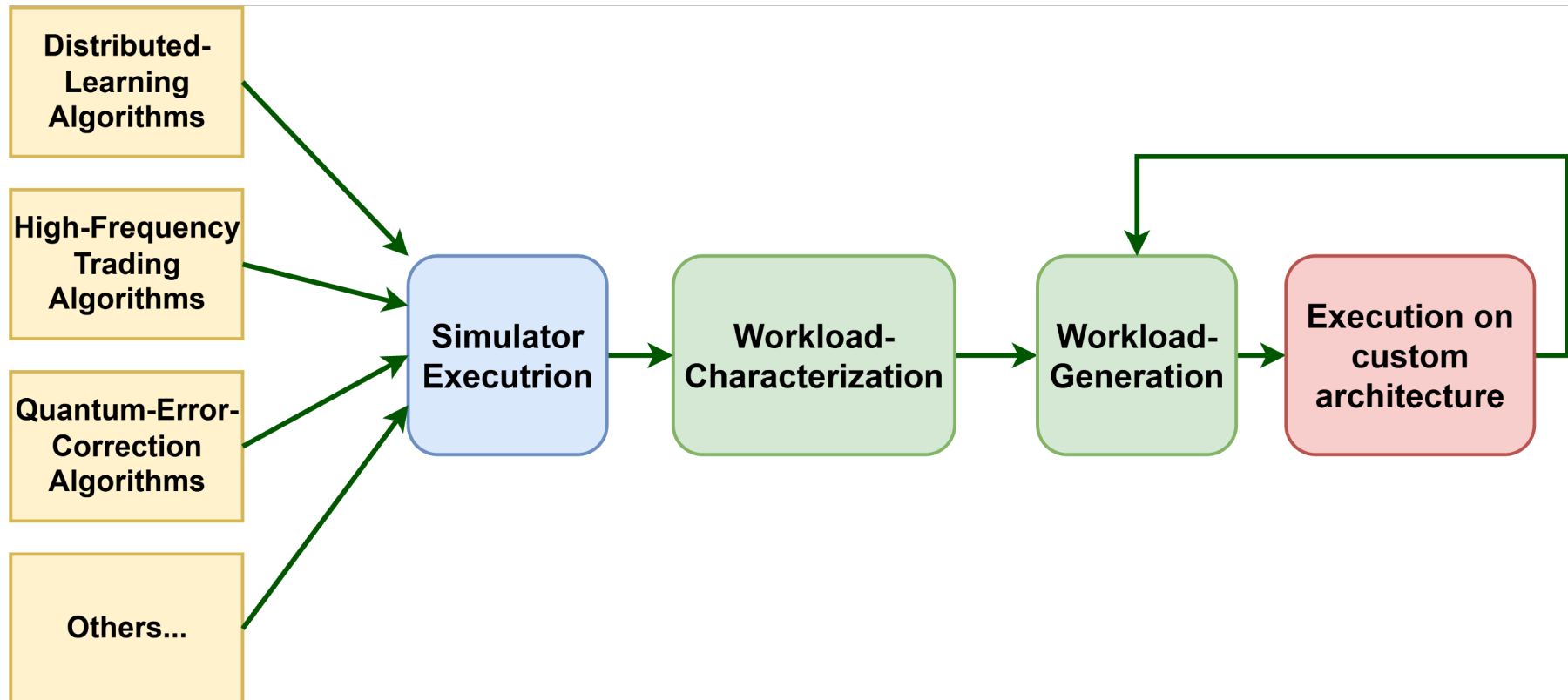


- **Objectives**

- Analyze and **characterize** the workload
- **Adapt** the hardware to execute that workload in the most efficient way

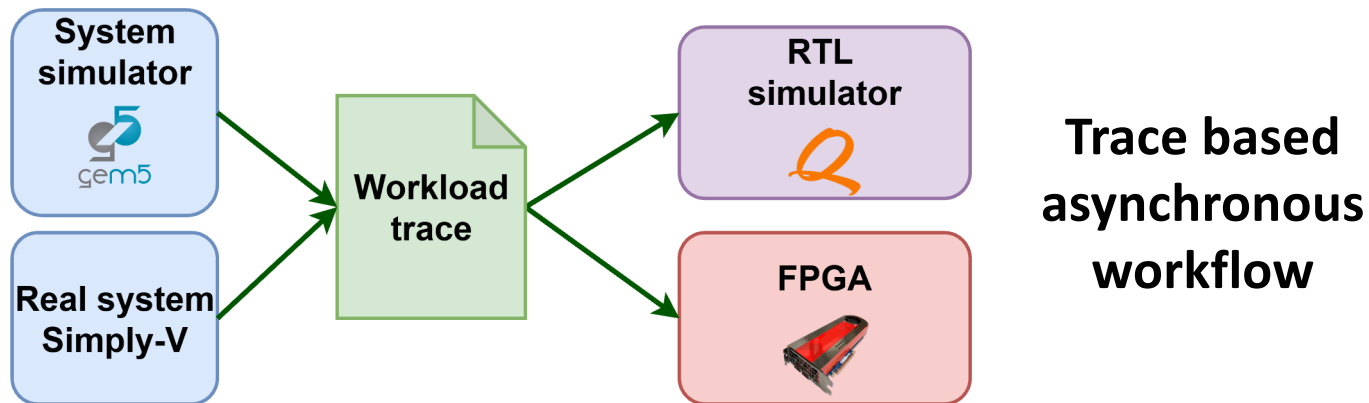
# Research Activity

- Methodology**



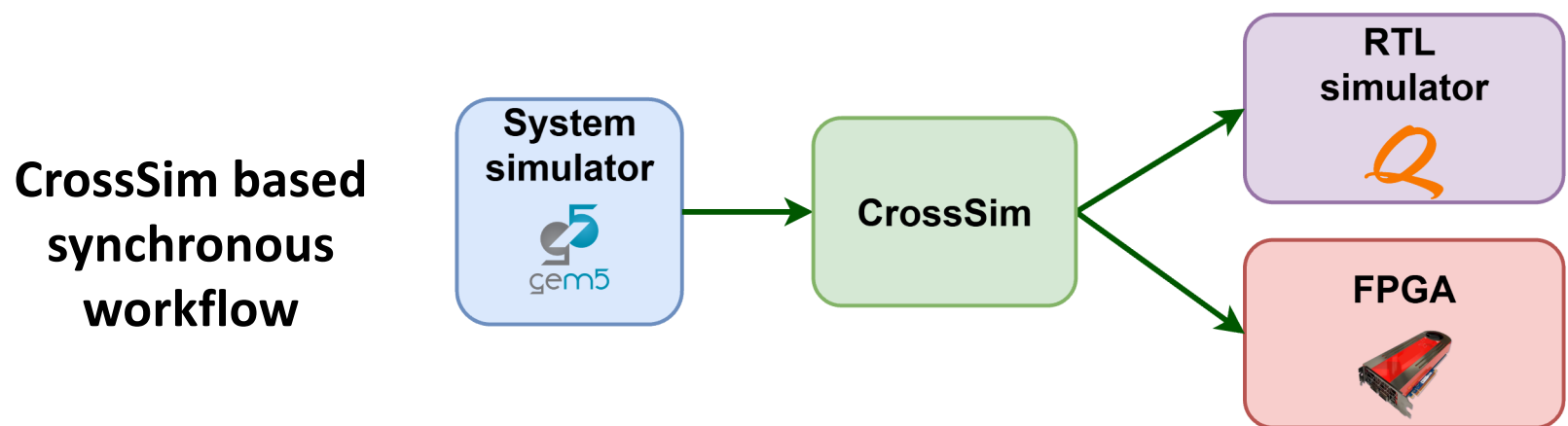
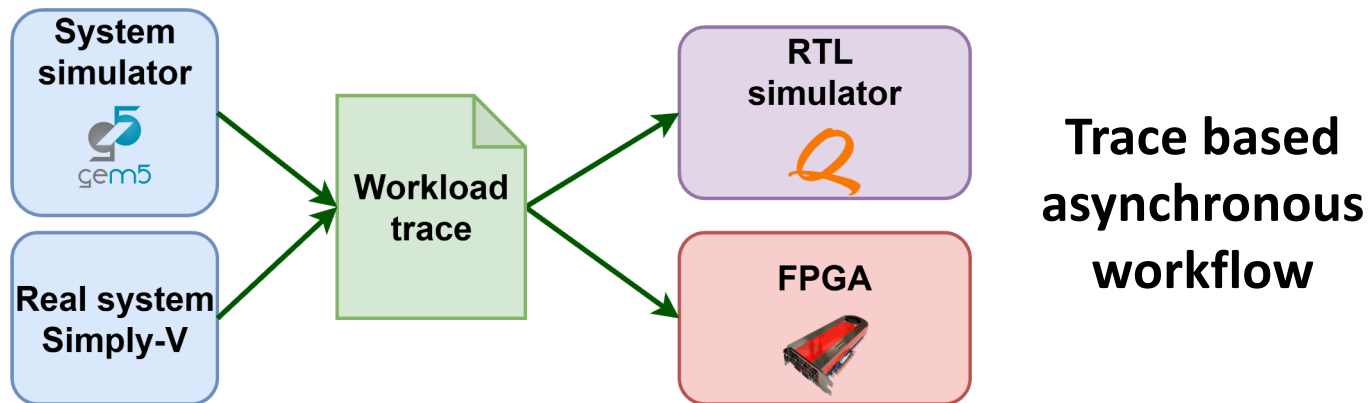
# Research Activity

- Methodology



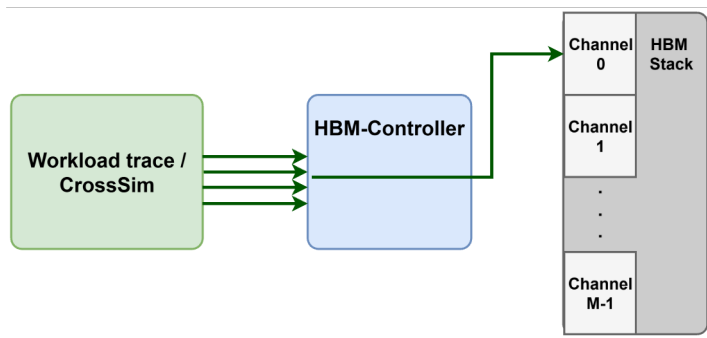
# Research Activity

- Methodology



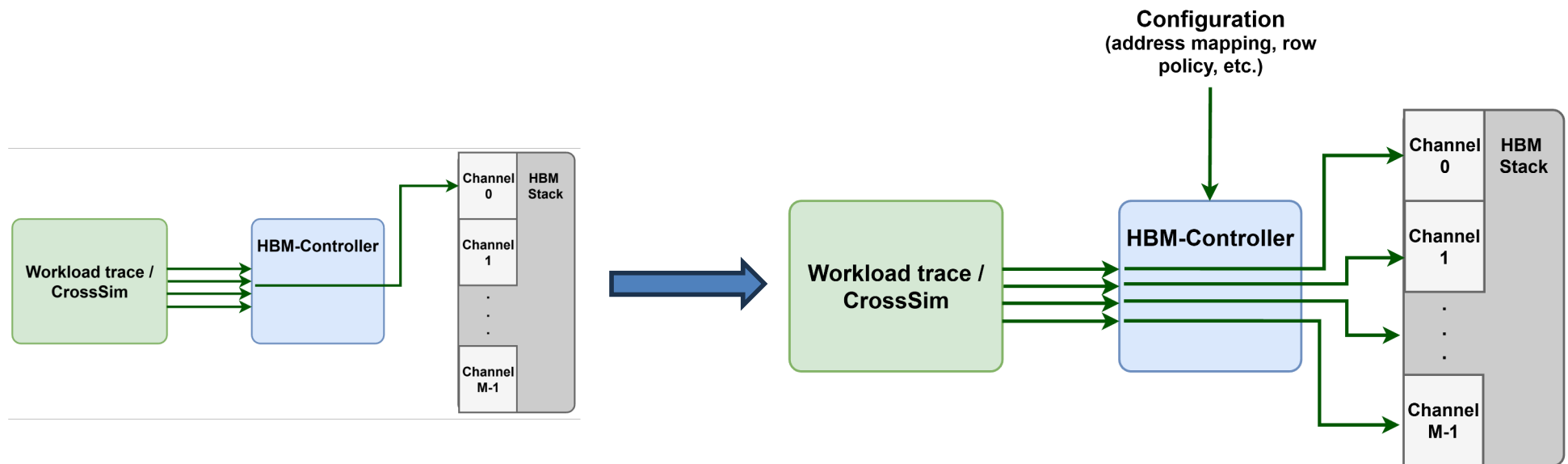
# Research Activity

- **Use case**
  - **Predictable/Customizable High-Bandwidth Memory (HBM) Controller.**
    - It can achieve **high performance** maintaining **predictability** guarantees.
    - I was able to turn it into a **customizable** architecture.



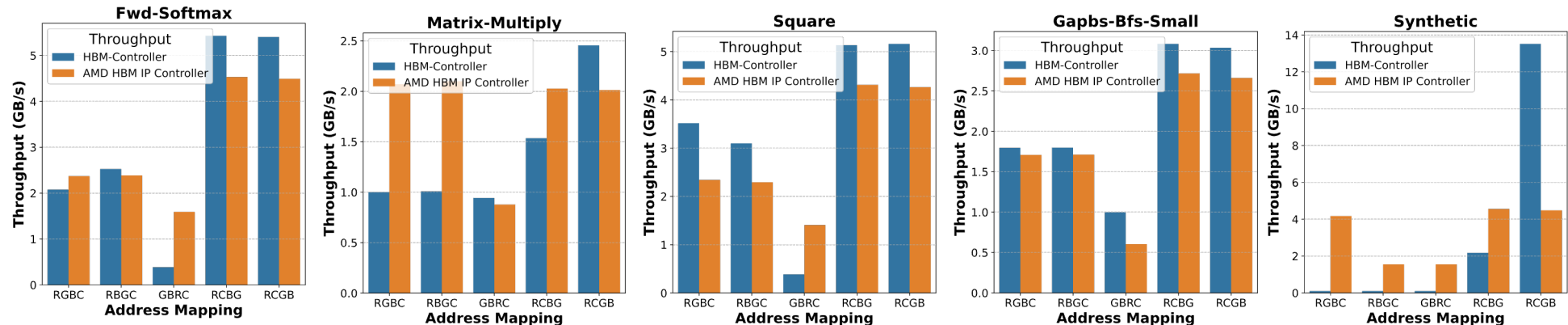
# Research Activity

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# Research results

- HBM Controller
  - Peak throughput of 13 GB/s per channel
  - An aggregate bandwidth of 416 GB/s
  - About 90% of the nominal bandwidth on AMD Alveo U280 card



# Research products

[P1]	Alessandro Cilaro, <b>Manuel Maddaluno</b> <i>Exploring time predictability for High-Bandwidth Memory technology</i> <b>IEEE Transactions on Emerging Topics in Computing</b> (ACCEPTED)
[E1]	Vincenzo Maisto, Stefano Mercogliano, <b>Manuel Maddaluno</b> , Alessandro Cilaro <i>Simply-V: A RISC-V Reconfigurable Playground Soft-SoC for Open Hardware Research and Fast Prototyping.</i> <b>WiPiEC Journal - Works in Progress in Embedded Computing Journal</b> (PUBLISHED)
[P2]	Vincenzo Maisto, Stefano Mercogliano, <b>Manuel Maddaluno</b> , Alessandro Cilaro <i>The Simply-V Framework: an Extensible RISC-V Reconfigurable Soft-SoC for Open Research and Fast Prototyping</i> <b>ACM Transactions on Design Automation of Electronic Systems</b> (SUBMITTED - Got Major Revision)
[P3]	Alessandro Cilaro, <b>Manuel Maddaluno</b> <i>A Customizable Open-Source HBM Controller</i> <b>ACM Transactions on Design Automation of Electronic Systems</b> (SUBMITTED)

E – Extended abstract; P – Regular paper

# What's next?

Extending the proposed methodology to other domains such as **distributed machine learning** and **quantum error correction**

Improving the proposed methodology adding **statistical workload characterization** and **generation** techniques

Applying the proposed methodology to an higher **system/rack level** not only to the microarchitectural.  
I will do that at **AMD in Dublin** during my **period abroad**