



UNIVERSITÀ DEGLI STUDI DI NAPOLI
FEDERICO II

itee_{PhD}
information technology
electrical engineering



Alberto Moriconi

An automatic methodology for the synthesis of approximate circuits

Tutor: Prof. Nicola Mazzocca

Cycle: XXXVII

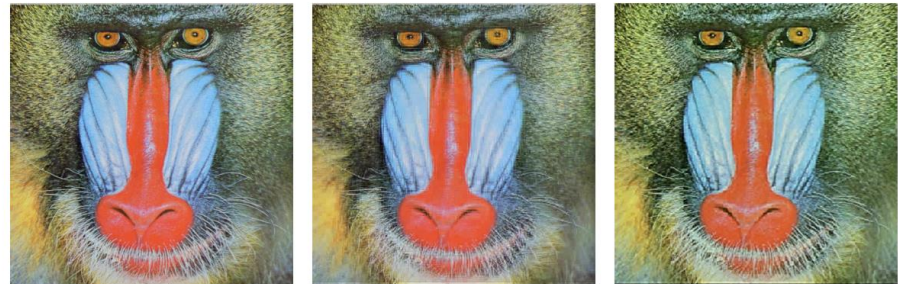
Year: 2023

My background

- MSc degree: Computer Engineering
- Research group/laboratory: Seclab / Embedded systems laboratory
- PhD start date: 1/11/2021
- Scholarship type: not funded

Research field of interest

- Amount of data to be processed is increasing, power consumption concerns are becoming increasingly critical.
- Approximate computing is a possible approach: we “gently” relax, in a controlled way, correctness requirements of specific applications (especially iterative or strictly tied to human perceptual limitations).
- In this way we can obtain area, time or power consumption advantages.



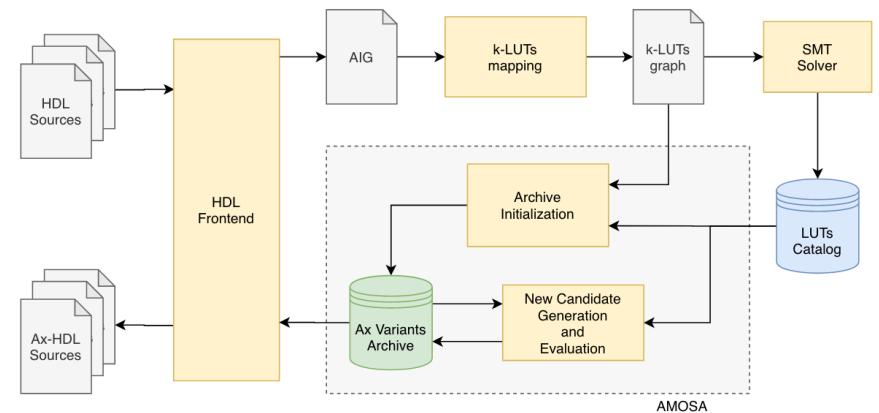
The well-known Baboon reference photo at different approximation levels

Summary of study activities

- Attended specific seminars on quantum computing, networking, machine learning and deep learning applications
- Attended and gave a technical presentation at:
 - ICSRS 2022

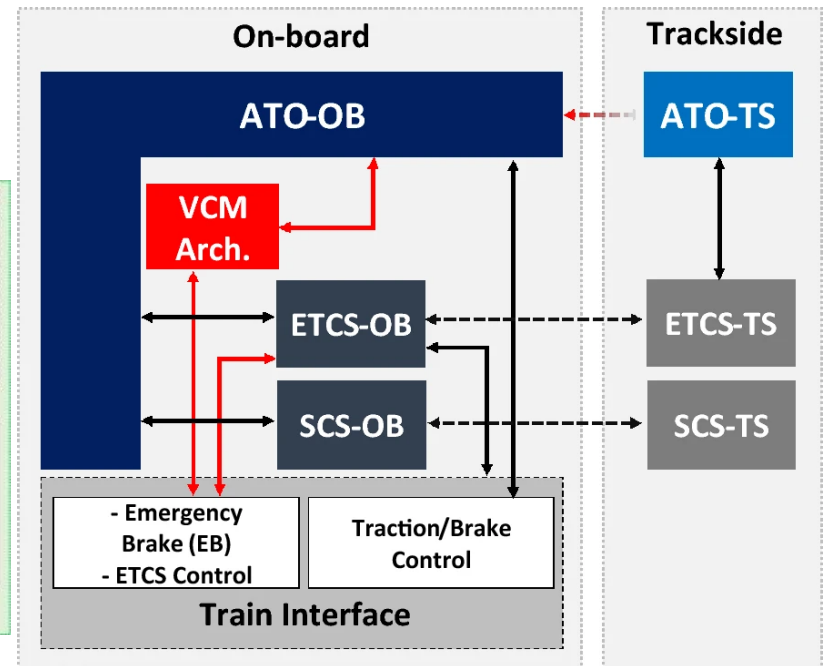
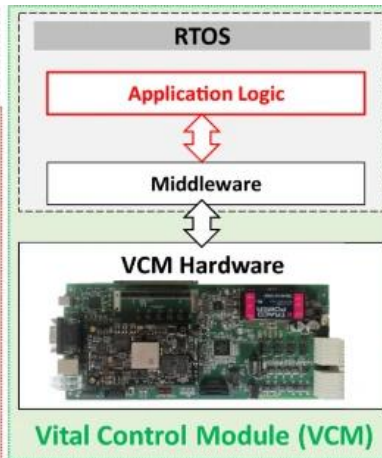
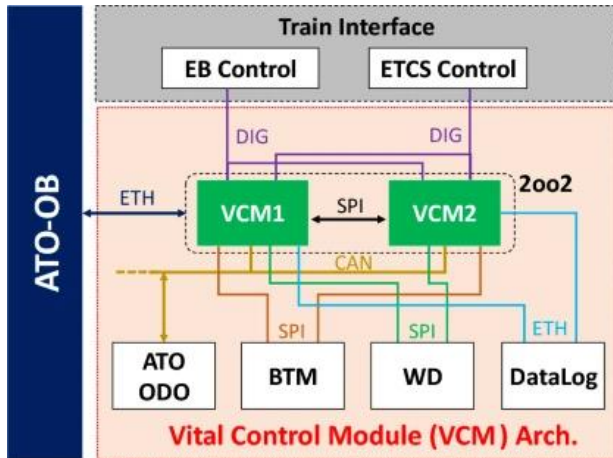
Research activity: Overview

- Problem (of your own research activity)
Devise an automatic and general methodology for the synthesis of approximate circuits.
- Objective
Provide an open-source implementation of a methodology that improves the current state-of-the-art for approximate combinatorial circuits synthesis.
- Methodology
Our methodology, based on the application of multi-objective combinatorial optimization to optimally selected cuts of combinatorial circuits, has been applied to well-known circuital benchmarks (i.e. real circuits used to test conventional synthesis suites), and the results has been compared to other approximation approaches.



Research activity: Overview

- Problem (of your own research activity)
Realize automatic train operation systems capable of achieving unsupervised operations on the mainlines.
- Objective
Identification and implementation of the additional safety functionalities that have to be provided.
- Methodology
Development of a model-based vital control module, implemented on a custom hardware architecture.



Products

[P1]	<p><i>M. Barbareschi, S. Barone, V. Casola, P. Montone and A. Moriconi, "A Memory Protection Strategy for Resource Constrained Devices in Safety Critical Applications," 2022 6th International Conference on System Reliability and Safety (ICSRS), Venice, Italy, 2022, pp. 533-538, doi: 10.1109/ICSRS56243.2022.10067350.</i></p> <p><i>Awarded Best presentation of its session.</i></p>
[P2]	<p><i>Amendola, A., Barbareschi, M., De Simone, S. et al. A real-time vital control module to increase capabilities of railway control systems in highly automated train operations. Real-Time Syst (2023).</i></p> <p><i>https://doi.org/10.1007/s11241-023-09401-5</i></p>
[P3]	<p><i>G. Mezzina et al., "A Step Toward Safe Unattended Train Operations: A Pioneer Vital Control Module," 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE), Antwerp, Belgium, 2023, pp. 1-4, doi: 10.23919/DATE56975.2023.10137186.</i></p>
[P4]	<p><i>Mezzina, G. et al. (2023). Model-Based Vital Control Architecture for Highly Automated Train Operations. In: Berta, R., De Gloria, A. (eds) Applications in Electronics Pervading Industry, Environment and Society. ApplePies 2022. Lecture Notes in Electrical Engineering, vol 1036. Springer, Cham. https://doi.org/10.1007/978-3-031-30333-3_21</i></p>
[P5]	<p><i>Barbareschi, M., Barone, S., Mazzocca, N., & Moriconi, A. "FPGA Approximate Logic Synthesis through Catalog-Based AIG-Rewriting Technique". (Journal paper, submitted)</i></p>

Next year

- Completing the analysis and characterization of the behavior of existing tools on FPGA synthesis.
- Based on the results of this step, devising a simplified methodology that is specifically aimed to the optimization of switching activity in LUT-based devices.
- Evaluate light-weight methods for metrics evaluation, such as algebraic methods for arithmetic circuits and signal-reliability analysis techniques from the circuit testing literature.
- Add other applicative examples to enrich the final thesis.

I would also like to explore other emerging technologies, especially those applicable in low-power and constrained-resources devices.