PhD in Information Technology and Electrical Engineering
Università degli Studi di Napoli Federico II

PhD Student: Vincenzo Maisto

Cycle: XXXVII

Training and Research Activities Report

Year: First

Vincenzo Maisto

Tutor: prof. Alessandro Cilardo

Alessandro Cilardo

Date: December 15th, 2022

Training and Research Activities Report

PhD in Information Technology and Electrical Engineering

Cycle: XXXVII **Author: Vincenzo Maisto**

1. Information:

- PhD student: Vincenzo Maisto
- DR number: DR995868
- Date of birth: 24/09/1996
- Master Science degree: Computer Engineering; University: University of Naples Federico II
- Doctoral Cycle: XXXVII
- Scholarship type: *MUR PON*
- Tutor: prof. Alessandro Cilardo

2. Study and training activities:

Activity	Type[1]	Hours	Credits	Dates	Organizer	Certificate[2]
Introduction to Quantum Circuits	Course	72	9	10/01/2022	Prof. Giovanni Miano	Y
Quantum Information	Course	48	6	18/01/2022	Prof. Angela Sara Cacciapuoti	Y
Virtualization technologies and their applications	Course	20	5	04/03/2022	Prof. Luigi De Simone	Y
Imprenditorialità Accademica	Course	16	4	14/06/2022	Prof. Pierluigi Rippa	Y
Big Data Analytics and Architectures	Course	18	5	07/11/2022	Prof. Giancarlo Sperlì	Y
The Spatial structure of Bi-photon States	Seminar	1	0,2	11/01/2022	P. Lucignano, D. Montemurro, D. Massarotti, V. D'Ambrosio, F. Cardano and M. Esposito	Y
Intelligenza artificiale e sistemi d'arma autonomi	Seminar	2	0.4	19/01/2022	Gruppo Interdisciplinare su Scienza, Tecnologia e Società (GISTS)	Y

					dell'Area della Ricerca di Pisa del CNR	
The quest of quantum advantage with a photonics platform	Seminar	1	0.2	03/02/ 2022	Scuola Superiore Meridionale	Y
Seeqc: the digital quantum computing company	Seminar	1	0.2	24/02/ 2022	P. Lucignano, D. Montemurro, D. Massarotti, V. D'Ambrosio, F. Cardano and M. Esposito	Y
Global and cluster synchronization in complex networks and beyond	Seminar	1	0.2	10/03/ 2022	Scuola Superiore Meridionale	Y
IEEE Authorship and Open Access Symposium: Tips and Best Practices to Get Published from IEEE	Seminar	1.5	0.3	30/03/ 2022	IEEE	Y
Analizzare i conflitti, costruire la pace: Ciberconflitti e minacce per la pace e la stabilità internazionale	Seminar	2	0.4	05/04/ 2022	Gruppo RUniPace UNINA	Y
An Introduction to Deep Learning for Natural Language Processing	Seminar	1	0.2	13/06/ 2022	Prof. Francesco Cotugno	Y
Switched differential algebraic equations: jumps and impulses	Seminar	1	0.2	01/06/ 2022	Prof. Raffaele Iervolino	Y
Probing and infusing biomedical knowledge for pre-trained language models	Seminar	2	0.4	07/06/ 2022	Prof. Francesco Cutugno	Y
Variable IO Latencies in real life	Seminar	2	0.4	09/06/ 2022	Prof. Marcello Cinque	Y
Quantum computing with superconducting	Seminar	1	0.4	20/06/ 2022	Procolo Lucignano,	Y

qubits, an overview on the current state and future directions at Rigetti computing					Domenico Montemurro, Davide Massarotti, Vincenzo D'Ambrosio, Filippo Cardano and Martina Esposito	
Introduction to Intellectual Property Management	Seminar	2	0.4	19/07/ 2022	5G Academy	Y
Software Engineering: Practical challenges and how researchers can help	Seminar	1.5	0.3	12/09/ 2022	QUATIC 2022 Conference	Y
Quality assessment of untestable programs: the metamorphic way	Seminar	1.5	0.3	13/09/ 2022	QUATIC 2022 Conference	Y
Recognizing Developers' Emotions: Advances and Open Challenges	Seminar	1.5	0.3	13/09/ 2022	QUATIC 2022 Conference	Y
Privacy-Preserving Machine Learning	Seminar	2	0.4	14/10/ 2022	Proff. Simon Pietro Romano, Roberto Natella	Y
Stabilizer Renyi Entropy and Quantum Complexity	Seminar	1	0.2	02/11/ 2022	Procolo Lucignano, Domenico Montemurro, Davide Massarotti, Vincenzo D'Ambrosio, Filippo Cardano and Martina Esposito	Y
Publishing Open Access IEEE Journal Articles under the Care Crui Agreement in Italy	Seminar	1	0.2	09/11/ 2022	IEEE	Y
Data mining the output of quantum simulators - from critical	Seminar	1	0.2	11/11/ 2022	Procolo Lucignano, Domenico	Y

behavior to algorithmic complexity					Montemurro, Davide Massarotti, Vincenzo D'Ambrosio, Filippo Cardano and Martina Esposito	
Complex network systems: introduction and open challenges	Seminar	2	0.4	17/11/ 2022	Scientific Colloquium at SSM	Y
Cybercrime and Information Warfare: National and International Actors	Seminar	2	0.4	18/11/ 2022	Proff. S.P. Romano, R. Natella	Y
Date 2022 Conference	Research	8	1.6	16-23/03/ 2022		N
Workshop Nazionale per il Trasferimento Tecnologico e l'Alta Formazione	Research	13.5	2.7	16-17/06/ 22	Laboratorio Embedded Systems & Smart Manufacturing	Y
QUATIC 2022 Conference	Research	15	3	12-14/09/ 22		Y

1) Courses, Seminar, Doctoral School, Research, Tutorship
2) Choose: Y or N

2.1. Study and training activities - credits earned

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	15	1	2	0	18
Bimonth 2	5	1.1	4	0	10.1
Bimonth 3	0	1.2	9	0	10.2
Bimonth 4	4	0.4	3	0	7.4
Bimonth 5	0	1.3	8	0	9.3
Bimonth 6	5	1.4	3	0	9.4
Total	29	6.4	29	0	64.4
Expected	30 - 70	10 - 30	80 - 140	0 – 4.8	

3. Research activity:

3.1. Topic

During this first year, my research activity focused on the construction of the base of knowledge and methodologies for innovative computing architectures, with a pivotal attention to heterogenous computing architectures. The main target is the sustainable acceleration of workloads from industry and academia with the adoption of cutting-edge technologies. Sustainability is addressed in terms of power consumption and scalability, alongside the improvement of timing performance. In this sense, I focused on modern Field Programmable Gate Array (FPGA) technology integrated in on-chip complex multi-processor systems, namely Multi-Processors System-on-Chips (MPSoCs).

3.1.1. Workloads and use cases

Applicative workloads and use cases have been identified among those of greater interest in the scientific community, i.e., Quantum Computing and Quantum Error Correction, Deep Learning and Artificial Intelligence. The collaboration with the company A3cube provided an HPC-oriented use case, i.e., erasure coding-based error correction, data compression, distributed file systems and computing paradigms for datacenter infrastructures.

3.1.2. Quantum Computing

Quantum computing and engineering are considered as fundamental tools in the foreseeable future. For this reason, during this year I spent a considerable effort in the study of the state-of-the-art and research directions in the field. The aim is to keep up to date with cutting-edge technologies and computing paradigm as they evolve, in order to propose meaningful contribution to the development of the field of quantum computing architectures.

3.2. Methodologies

3.2.1. Hardware/software Co-design and MPSoCs

MPSoC platforms offer the possibility to perform advanced hardware-software codesign and to perform fine-grain design, engineering and aggressive optimizations for target workloads and application use cases. Furthermore, tight on-chip integration of CPUs and FPGA fabric greatly reduces power-consumption by reducing the need for off-chip data-movement. With the aim of reaching a deep technological understanding of such platforms, I experimented and tested advanced FPGA design technologies, like dynamic partial reconfiguration, floorplanning, High Level Synthesis (HLS) and OpenCL-based synthesis, alongside with their software engineering use and perspective. Such experience was acquired on the hardware platforms and software environments of both leading FPGA vendors, namely Xilinx and Intel, formerly Altera.

3.2.2. Linux Device Drivers

With reference to the software-oriented activities of the hardware/software co-design methodology, the pivotal technologies I faced and addressed during this first year were Linux device drivers and Linux kernel development. Although user-level libraries offer the fundamental APIs to the final user, the core of the co-design activity is in the engineering of kernel modules and device drivers for FPGA integrated hardware design and co-processors. During this first year, I addressed several advanced drivers and frameworks in the Linux kernel, namely Linux FPGA manager, PCIe drivers, platform devices and the Linux tracing infrastructure.

3.3. Results

Experimentation targeted both resource-limited edge-class and powerful server/HPC-class MPSoCs.

3.3.1. Edge Computing

Most of the experimental effort of this first year was on edge-class systems. I targeted Xilinx Zynq UltraScale+ edge-class MPSoCs. At first, I performed an extensive analysis of the platform and the technologies it features. I evaluated the possibility to floorplan and perform dynamic partial configuration of complex designs on such a resource-limited platform. Together with the other authors, in the paper "A Proposal for FPGA-Accelerated Deep Learning Ensembles in MPSoC Platforms Applied to Malware Detection", I proposed a hardware/software architecture, featuring edge-class MPSoCs as technological platform and leveraging virtualization technologies to enforce security-related requirements and performing a preliminary security analysis to increase the security-by-design of the proposed architectures. Subsequently, I designed a systematic methodology for the characterization of a multitask Deep Learning applications. I applied such methodology to complex black-box configurable Deep Learning coprocessor IP for FPGAs provided by Xilinx, namely the Deep Learning Processing Unit (DPU). Results are presented in the currently under review paper "An approach to the systematic characterization of multitask accelerated AI inference in edge MPSoCs". As a summary, the findings of the application of the systematic methodology were meaningful insights on the scheduling and allocation policy of software threads on hardware threads of the co-processor and the reverse-engineering of some debug performance counters of the black-box IP, and finally, an energy consumption estimation based only on the data collected during the multitasking performance evaluation.

3.3.2. HPC

Regarding HPC and server-class MPSoCs, the targets of my research are Intel data-center Programmable Acceleration Cards (PACs). In particular, current target devices are Intel Rush Creek architectures featuring Arria10 FPGAs and the novel Intel Agilex platforms. Analysis and the experimental campaign on such platforms started in the last months of this year and are currently work in progress.

4. Research products:

1) *V. Maisto and A. Cilardo, "A Pluggable Vector Unit for RISC-V Vector Extension", doi: 10.23919/DATE54114.2022.9774501 [published];*
2) *Cilardo, A., Maisto, V., Mazzocca, N., Rocco di Torrepadula, F. (2022). A Proposal for FPGA-Accelerated Deep Learning Ensembles in MPSoC Platforms Applied to Malware Detection. doi: https://doi.org/10.1007/978-3-031-14179-9_16 [published].*
3) *Cilardo, A., Maisto, V., Mazzocca, N., Rocco di Torrepadula, F. . An approach to the systematic characterization of multitask accelerated AI inference in edge MPSoCs [Submitted on October 31st, 2022, to ACM TECS (Transactions on Embedded Computing Systems)]*

5. Conferences and seminars attended

1) *DATE 2022: Design Automation and Test in Europe:*
   a. *Presentation of above conference paper "A Pluggable Vector Unit for RISC-V Vector Extension";*

2) *Workshop Nazionale per il Trasferimento Tecnologico e l'Alta Formazione 2022 organized by the Embedded Systems & Smart Manufacturing (ESSM) Laboratory:*
    a. *Presentation of the tutorial "Edge AI on FPGAbased MPSoC devices";*
    b. *Presentation of the poster "Towards the acceleration of AI on MPSoC embedded systems and open platforms";*
3) *QUATIC 2022, 15th International Conference on the Quality of Information and Communications Technology:*
    a. *Presentation of the above conference paper "A Proposal for FPGA-Accelerated Deep Learning Ensembles in MPSoC Platforms Applied to Malware Detection"*

6. Activity abroad:

None

7. Tutorship

None