UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

DOTTORATO DI RICERCA / PHD PROGRAM IN
INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

Activities and Publications Report

PhD Student: Vincenzo Maisto

Student DR number: DR995868

PhD Cycle: XXXVII
PhD Cycle Chairman: Prof. Stefano Russo

PhD program student's start date: 01/01/2022
PhD program student's end date: 31/12/2024

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PhD scholarship funding entity: MUR PON and University of Naples Federico II

General information

Vincenzo Maisto received in year 2020 the Master Science degree in Computer Engineering from the University of Napoli Federico II. He attended a curriculum in Computer Engineering subject within the PhD program in Information Technology and Electrical Engineering. He received a grant from Università Federico II.

Study activities

Attended Courses

Year	Course Title	Type	Credits	Lecturer	Organization
1st	Virtualization Technologies and their applications	Ad hoc course	5	Luigi De Simone	ITEE
1st	Imprenditorialità accademica	Ad hoc course	4	Pierluigi Rippa	ITEE
1st	Big Data Analytics and Architectures	Ad hoc course	5	Giancarlo Sperlì	ITEE
1st	Introduzione ai Circuiti Quantistici	MSc course	9	Giovanni Miano	University of Naples Federico II
1st	Quantum Information	MSc course	6	Angela Sara Cacciapuoti	University of Naples Federico II
2nd	Statistical data analysis for science and engineering research	Ad hoc course	4	Roberto Pietrantuono	University of Naples Federico II
3rd	Strategic Orientation for STEM Research & Writing	Ad hoc course	5	Chie Shin Fraser	ITEE

Attended PhD Schools

None

Attended Seminars

Year	Seminar Title	Credits	Lecturer	Lecturer affiliation	Organization
1st	Seeqc: the digital quantum computing company	0.2	Marco Arzeo	Seeqc-EU srl	University of Napoli Federico II
1st	Intelligenza artificiale e sistemi d'arma autonomi	0.4	Fosca Giannotti, Guglielmo Tamburrini	University of Napoli Federico II	Gruppo interdisciplinare su scienza, tecnologia e società dell'area della ricerca di Pisa del CNR
1st	The special structure of bi-photon states	0.2	Alessio D'Errico	University of Ottawa	University of Napoli Federico II

1st	The quest of quantum advantage with a photonics platform	0.2	Fabio Sciarrino	University of Rome La Sapienza	Scuola Superiore Meridionale
1st	IEEE Authorship and Open Access Symposium: Tips and Best Practices to Get Published from IEEE	0.3	Dr. Derek Abbott, Dr. Paolo Bonato, Eszter Lukács, Judy Brady	N/A	IEEE
1st	An introduction to deep learning for natural language processing	0.2	Marco Valentino	N/A	ITWW
1st	Global and cluster synchronization in complex networks and beyond	0.2	Mattia Frasca	Università di Catania	Scuola Superiore Meridionale
1st	Analizzare i conflitti, construire la pace: ciberconflitti e minacce per la pace e la stabilità internazionale	0.4	Simon Pietro Romano, Guglielmo Tamburrini	University of Napoli Federico II	Gruppo REUniPace UNINA
1st	Quantum computing with superconducting qubits, an overview on the current state and future directions at Rigetti computing	0.2	Stefano Poletto	Righetti Computing	University of Napoli Federico II
1st	Variable IO Latencies in real life	0.4	Luca Porzio, Roberto Izzi, Dionisio Minopoli	Micron Semiconductor Italia S.r.l.	University of Napoli Federico II
1st	Probing and infusing biomedical knowledge for pre-trained language models	0.4	Zaiqiao Meng	University of Glasgow	ITEE
1st	Switched differential algebraic equations: jumps and impulses	0.2	Stephan Trenn	University of Groningen	ITEE
1st	Introduction to Intellectual Property Managemen	0.4	Alessandro Marroni	NOKIA	5G Academy
1st	Software Engineering:	0.3	Mauricio	TU Delft	QUATIC 2022 Conference

	Practical challenges and how researchers can help		Aniche		
1st	Recognizing Developers' Emotions: Advances and Open Challenges	0.3	Nicole Novielli	University of Bari	QUATIC 2022 Conference
1st	Quality assessment of untestable programs: the metamorphic way	0.3	Sergio Segura	University of Seville	QUATIC 2022 Conference
1st	Privacy-preserving Machine Learning	0.4	Vittorio Podromo	N/A	University of Napoli Federico II
1st	Cybercrime and information warfare: national and international actors	0.4	Pierluigi Pagani	N/A	University of Napoli Federico II
1st	Complex network systems: introduction and open challenge	0.4	Pietro De Lellis	University of Napoli Federico II	Scuola Superiore Meridionale
1st	Data mining the output of quantum simulators - from critical behavior to algorithmic complexity	0.2	Marcello Dalmonte	Abdus Salam ICTP Trieste	University of Napoli Federico II
1st	Publishing Open Access IEEE Journal Articles under the Care Crui Agreement in Italy	0.2	Eszter Lukacs	IEEE	IEEE
1st	Stabilizer Renyi Entropy and Quantum Complexity	0.2	Alioscia Hamma	University of Napoli Federico II	University of Napoli Federico II
2nd	The state of the art of AI and Physics-Based Simulations in drug discovery	0.2	Andrea Beccary	Dompè	University of Napoli Federico II
2nd	How to Publish Under the CARE-CRUI Open Access Agreement with IEEE	0.3	Nino Grizzuti, Eszter Lukacs, Stefano Bianco	CARE-CRUI and IEEE	CARE-CRUI and IEEE
2nd	Enhancing qubit readout with Bayesian Leaning	0.2	Nicola Lo Gullo	University of Calabria	University of Napoli Federico II
2nd	Unleashing the power of LLMs: a historical perspective on	0.2	Tarry Singh	Real AI Inc.	ITEE

	generative AI				
2nd	Integrated Systems Seminars	0.75	Luca Benini, Georg Rutishauser, Cristi Ciofaln and others	ETH Zurich	External seminar at ETH IIS (Integrated Systems Laboratory), Zurich, Switzerland
2nd	Exploring Advanced Aerial Robotics: A Journey into CuttingEdge Projects and Neural Control	0.2	Eugenio Cuniato	ETH Zurich	ITEE
2nd	Traffic Engineering with Segment Routing: optimally dealing with most popular use-cases	0.2	Pascal Mérindol	Université de Strasbourg, France	ITEE
2nd	DaeMon: Architectural Support for Efficient Data Movement in Disaggregated Memory Systems	0.2	Christina Giannoula	University of Toronto	External seminar at SAFARI ETH Zurich, Zurich, Switzerland
2nd	A RISC-V Vector-Processor for High-throughput Multidimensional Sensor Data Processing	0.4	Matteo Perotti	ETH Zurich	External seminar at ETH Future Computing Laboratory, Zurich, Switzerland
2nd	Economic Fitness Concepts, Methods and Applications	0.3	Luciano Pietronero	University of Roma "La Sapienza", Rome, Italy	Scuola Superiore Meridionale
2nd	Deep Learning for Railway Safety and Maintenance: Methodologies and Applications	0.3	Lorenzo De Donato	DIETI, UNINA	DIETI, UNINA
3rd	I finished my PhD, but what can I do now? The MarieSklodowska Curie Actions	0.2	Dr Narciso M. Quijada	University of Salamanca, Spain	DEPARTMENT OF AGRICULTURAL SCIENCES, UNINA
3rd	Causality Tracing and Root Cause Analysis with Visualizer	0.2	Hari Gurrala, Jerome Burke	Siemens EDA	External seminar at Siemens EDA Customer Support Expert Series webinar (https://eda.sw.siemens.com/en-US/eda-events/)

3rd	Edoardo Giusto research past, present and future	0.2	Edoardo Giusto	DIETI, UNINA	DIETI, UNINA

Research activities

Vincenzo Maisto participated in several research activities concerning computer architectures and energy efficiency. His research effort spanned the diverse landscape of digital computing domains, in search for common approaches for performance and hardware consolidation.

High Performance Computing

In the domain of HPC, Vicenzo Maisto, in collaboration with the partner company A3cube Inc., addressed the issue of energy efficient acceleration of erasure coding system workloads in Hadoop Distributed File System (HDFS).

He successfully integrated PCIe-attached FPGA acceleration, consolidating HDFS' multi-threaded workloads on a single device per HDFS cluster.

Edge-AI

In the field of edge-AI, he took interest in consolidating multi-tenant and multi-user workloads on edge-class MPSoC platforms.

He evaluated the multi-threaded scalability of AMD Xilinx Vitis-AI platform, unveiling energy inefficiency and scheduling limitations. Subsequently, he proposed the multi-DPU architecture, leveraging hardware heterogeneity and neural network scheduling with accelerator affinity.

Low Power SoCs

As a joint effort with his hosting research group at ETH Zurich, Vincenzo enabled micro-architectural virtual memory and operating system support for an open-source vector co-processor, namely PULP's Ara. This effort was crucial to enable hardware consolidation of vector applications through multi-threading.

He benchmarked Ara's multi-threading capabilities, successfully consolidating parallel computation at increased performance and energy efficiency.

Low Carbon Knowledge Distillation

Vincenzo Maisto also took part in the definition of low carbon training methodologies for low-footprint neural networks. He complemented the knowledge distillation model compression technique with a heuristic approach for energy-driven search space reduction for the compression hyperparameters.

Tutoring and supplementary teaching activities

Tutoring MSc Theses in topic of High-Performance Computing architectures, high-level design methodologies and virtualization-based hardware consolidation.

Credits summary

PhD Year	Courses	Seminars	Research	Tutoring / Supplementary Teaching
1st	29	6.4	29	0
2nd	4	3.25	49	0
3rd	5	0.6	53.75	0

Research periods in institutions abroad and/or in companies

PhD Year	Institution / Company	Hosting tutor	Period	Activities
2nd	ETH Zurich	Luca Benini	01/05/2023 – 31/10/2023	• Implementation of virtual memory support for open-source RISC-V vector co-processor, namely Ara • Integration of Ara co-processor in Linux-capable MPSoC, namely Cheshire • FPGA-prototyping of Cheshire SoC Linux support and benchmarking for RISC-V vector extension • Benchmark and validation of Ara's multi-threaded capabilities
1st- 3rd	A3cube Inc.	Emilio Billi	6 moths across 01/01/2022 – 31/12/2024	• Hardware acceleration for erasure coding through Intel HLS and OneAPI/SYCL • Architectural design and prototyping of multi-threaded hardware support package for Intel Agilex FPGAs • Architectural design and prototyping of software thread-isolation middleware for hardware resource proxying • Architectural design and prototyping of FPGA-acceleration for Hadoop Distributed File System

PhD Thesis

Computing technologies are nowadays ubiquitous and their demand is expanding at an ever-increasing rate. The environmental footprint of such immense growth is a severe environmental issue, with computational services alone expected to account for 20% of the global energy demand by 2030. Therefore, the interest in green computing approaches is rising, from low carbon methodologies, low power and energy efficient architectures, to water consumption awareness for datacenters. The modern digital computing landscape is extremely diverse and heterogeneous, with dissimilar requirements in scale and nature. High-end cloud systems are cluster-based and business-oriented, edge and IoT devices focus on field deployment and battery power, while low power SoC and CPU design is concerned with micro-architectural optimizations and power limits. Nevertheless, different domains share a common and pressing urge for lower energy consumption, either to save on the datacenter energy bill or prolong battery lifetime. On the other hand, the extreme diversity brings substantial challenges to common approaches. Most techniques are domain-specific and non-generalizable, common approaches are challenging to find and deploy, and there seems to be no silver bullet to save energy.

In the quest for energy efficiency across domains, this thesis presents and validates common approaches for energy efficiency and hardware consolidation across the digital computing landscape. We target server-class clusters, edge MPSoC platforms and low power SoC and CPU design. In search of common approaches, we avoid domain-specific methodologies that would not generalize across domains. Conversely, we enable hardware consolidation with advanced hardware/software co-design, scalability, and heterogeneity.

Research products

Research results appear in 1 paper published in international journals, 2 contributions to international conferences, and several others works currently under review in international journals and papers.

List of scientific publications

International journal papers

Alessandro Cilardo; Vincenzo Maisto; Nicola Mazzocca; Franca Rocco di Torrepadula
"An approach to the systematic characterization of multitask accelerated CNN inference in edge MPSoCs",
ACM Transactions on Embedded Computing Systems,
vol. 23, 3, Article 48 (May 2024), 25 pages. https://doi.org/10.1145/3611015.

Franca Rocco di Torrepadula; Vincenzo Maisto; Alessandro Cilardo; Nicola Mazzocca
"Distilling Knowledge for Low-Carbon AIoT",
IEEE Transactions on Sustainable Computing,
[submitted to ITEE Transactions on Sustainable Computing (TSUSC)]

International conference papers

Vincenzo Maisto, Alessandro Cilardo
"A Pluggable Vector Unit for RISC-V Vector Extension",
2022 Design, Automation & Test in Europe Conference & Exhibition (DATE),
Antwerp, Belgium, 2022, pp. 1143-1148, doi: 10.23919/DATE54114.2022.9774501.

Alessandro Cilardo; Vincenzo Maisto; Nicola Mazzocca; Franca Rocco di Torrepadula,
"A Proposal for FPGA-Accelerated Deep Learning Ensembles in MPSoC Platforms Applied to Malware Detection",
Quality of Information and Communications Technology. QUATIC 2022,
Talavera de la Reina, Spain, September 12–14, 2022, Springer Cham, DOI: https://doi.org/10.1007/978-3-031-14179-9_16.

Vincenzo Maisto, Alessandro Cilardo, Emilio Billi and Chuck Fader,
"A Hardware/Software Architecture for Multi-threaded Offloading of Erasure Codes in Distributed File Systems",
[submitted to International Symposium on Computer Architecture (ISCA) 2025]

V. Maisto and A. Cilardo,
"Multi-DPU: an Energy-efficient Hardware/Software Architecture for Multi-tenant Deep Learning Acceleration on Edge MPSoCs",
[submitted to Design, Automation and Test in Europe Conference (DATE) 2025]

Date 16/12/2024

PhD student signature Vincenzo Maisto

Supervisor signature

Firmato digitalmente da

Alessandro CILARDO

CN = CILARDO Alessandro
O = Università degli Studi di Napoli Federico II