Marco Vitone

Development of innovative techniques and methodologies for analysis and testing of Storage Systems interfaces based on System on Chip

Tutor: Prof. Nicola Petra co-Tutor: Eng. Claudio Giaccio

Cycle: XXXVI Year : 3

Background information

- MSc degree in Electronics Engineering at University of Naples Federico II
- Research group/laboratory : VLSI Electronics
- PhD start and end dates : 1/11/2020 – 31/10/2023
- Scholarship type: founded by Micron Semiconductor Italia S.R.L.
- Cooperation : Micron Hardware Validation Tool Team

Summary of study activities

- **Ad hoc courses**: Digital Forensics' methods practices and tools, Data Science for Patient Record Analysis , Scientific Programming and Visualization with Python, Statistical Data Analysis for Science and Engineering Research, Imprenditorialità Accademica, Cambridge English Preliminary (PET), Strategic Orientation for STEM Research & Writing.

- **MSc courses:** FPGA per l'elaborazione dei segnali, Dispositivi e Sistemi Fotovoltaici.

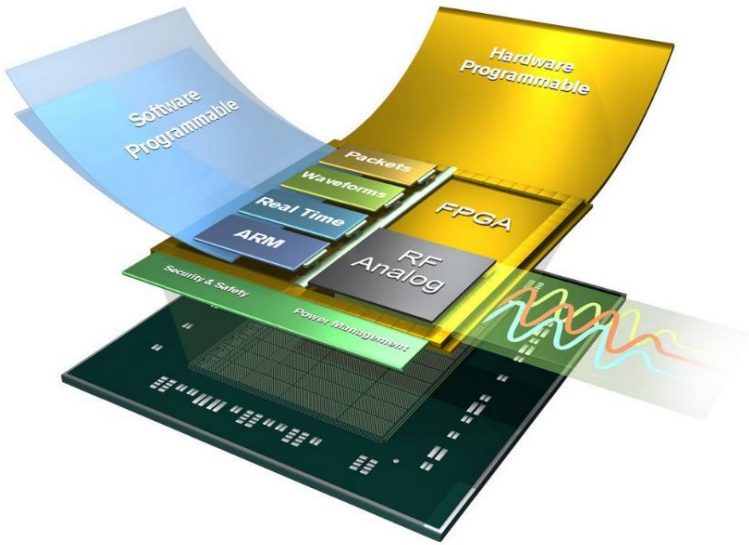
- **PhD School:** "Electronics for IoT", SIE Associazione Società Italiana di Elettronica, Trieste, 5-7/7/2021.

- **Credits Summary:**

PhD Year	Courses	Seminars	Research	Tutoring / Supplementary Teaching
1st	32.9	10.7	23.6	0
2nd	15	7.1	37.9	0
3rd	0	0	60	0

Research area

- **System on Chip** is a complex IC that integrates CPU, on-chip memory, programmable logic (FPGA) on a single chipset.
- **Applications**: signal processing, communication, networking, automotive, storage system management.
- **Problems:**
  - **Validation :** system level simulations, protocol interfaces analysis, etc.
  - **Design :** hardware accelerator, firmware development, peripherals management, etc.



Research results

- My research can be divided into **two main activities**.

- **Validation and debug** of complex SoC designs:

  - Implementation of **simulation environment** for a complex SoC devices adopting the **Universal Verification Methodology (UVM)**.
  - Development of an **innovative hardware emulation technique** that aims at introducing the **hardware in the loop** inside the validation of complex systems based on SoC platform.

- **Design of hardware accelerator** for SoC devices:

  - Implementation of a **novel FFA algorithm** for efficient hardware implementation of convolution.
  - Development of a **hardware data path** for the acceleration **of Convolutional Neural Networks (CNN).**

Research products

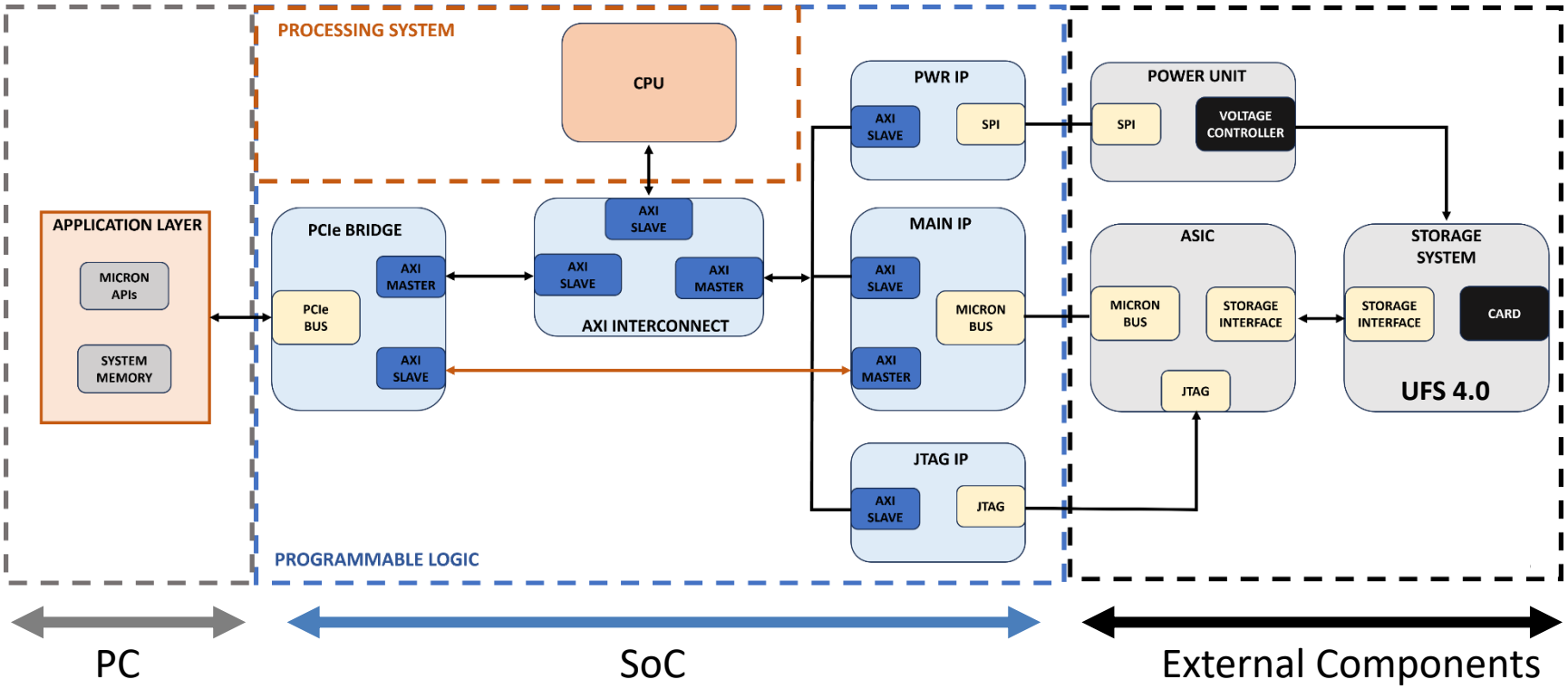
[C1]	M.Vitone, N.Petra *Reconfigurable Datapath for Hardware Acceleration of Convolutional Neural Network* 52nd Annual Meeting of Associazione Società Italiana di Elettronica (SIE) Trieste,Italy, Jult 2021

PhD thesis overview: validation and debug

- **Problem statement:**
  - Validation of the Micron system (digital, complex, SoC + ASIC)
- **Objective:**
  - Validation using Universal Verification Methodology (UVM)
  - UVM architecture with reduced execution time
  - Emulation architecture with hardware in the loop

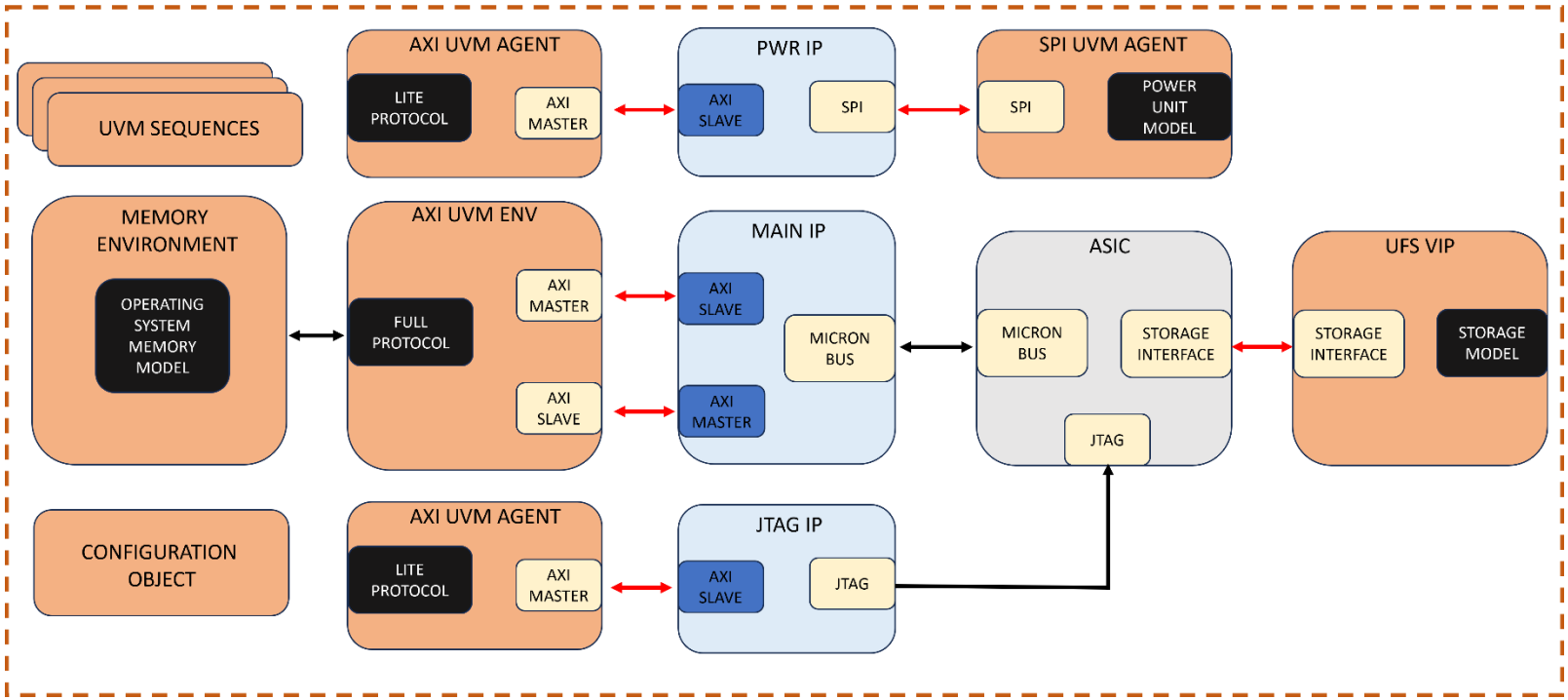
PhD Thesis: validation and debug

Micron Architecture: **PC + SoC + ASIC + UFS**



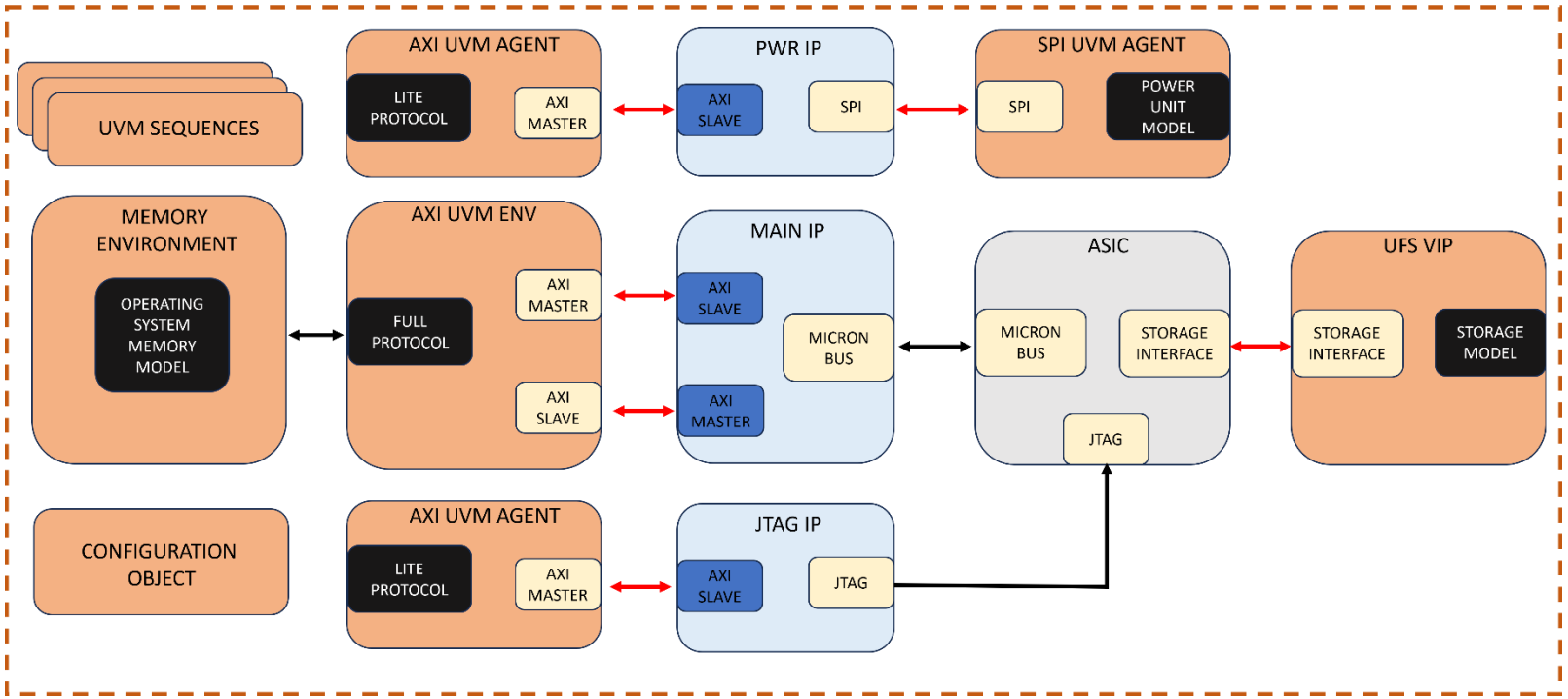
PhD Thesis: validation and debug

UVM ARCHITECTURE



PhD Thesis: validation and debug

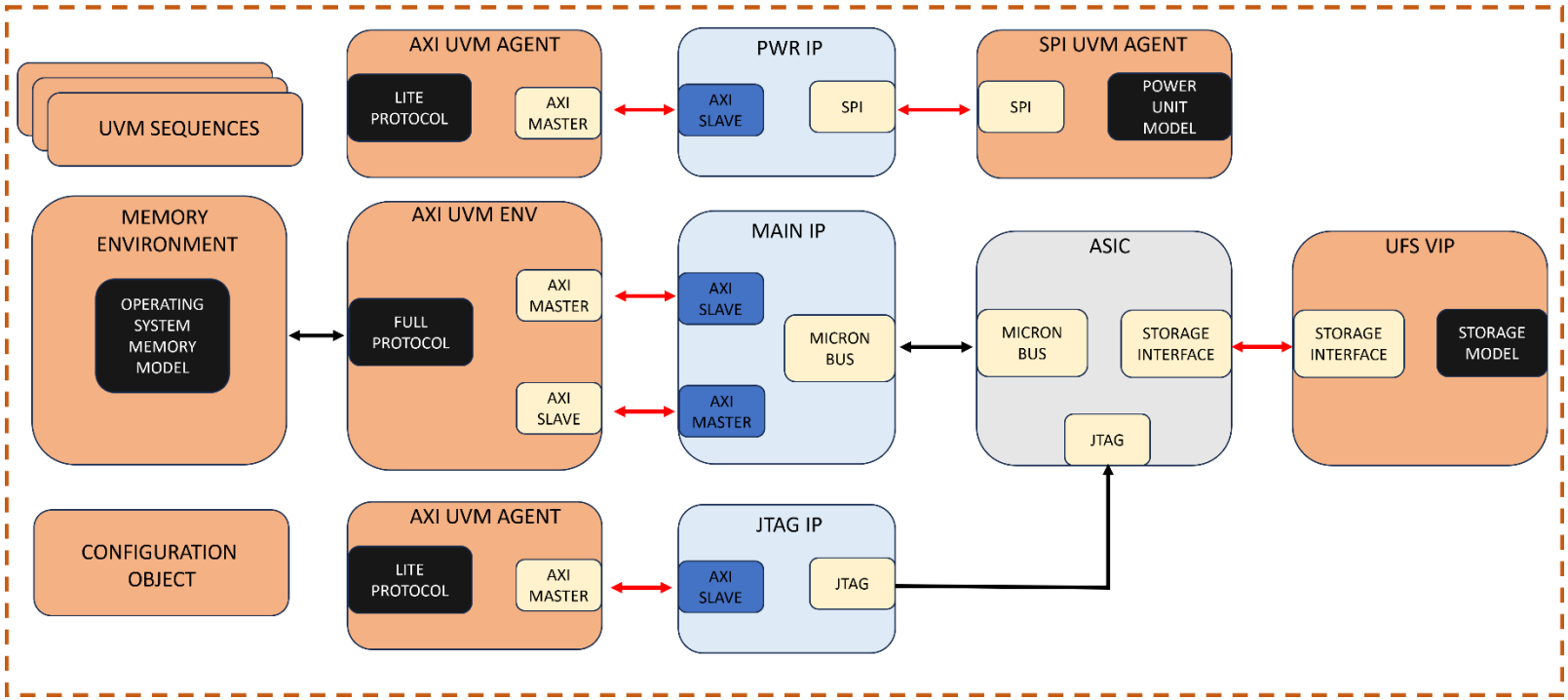
UVM ARCHITECTURE



Compliant standard UVM

PhD Thesis: validation and debug

UVM ARCHITECTURE

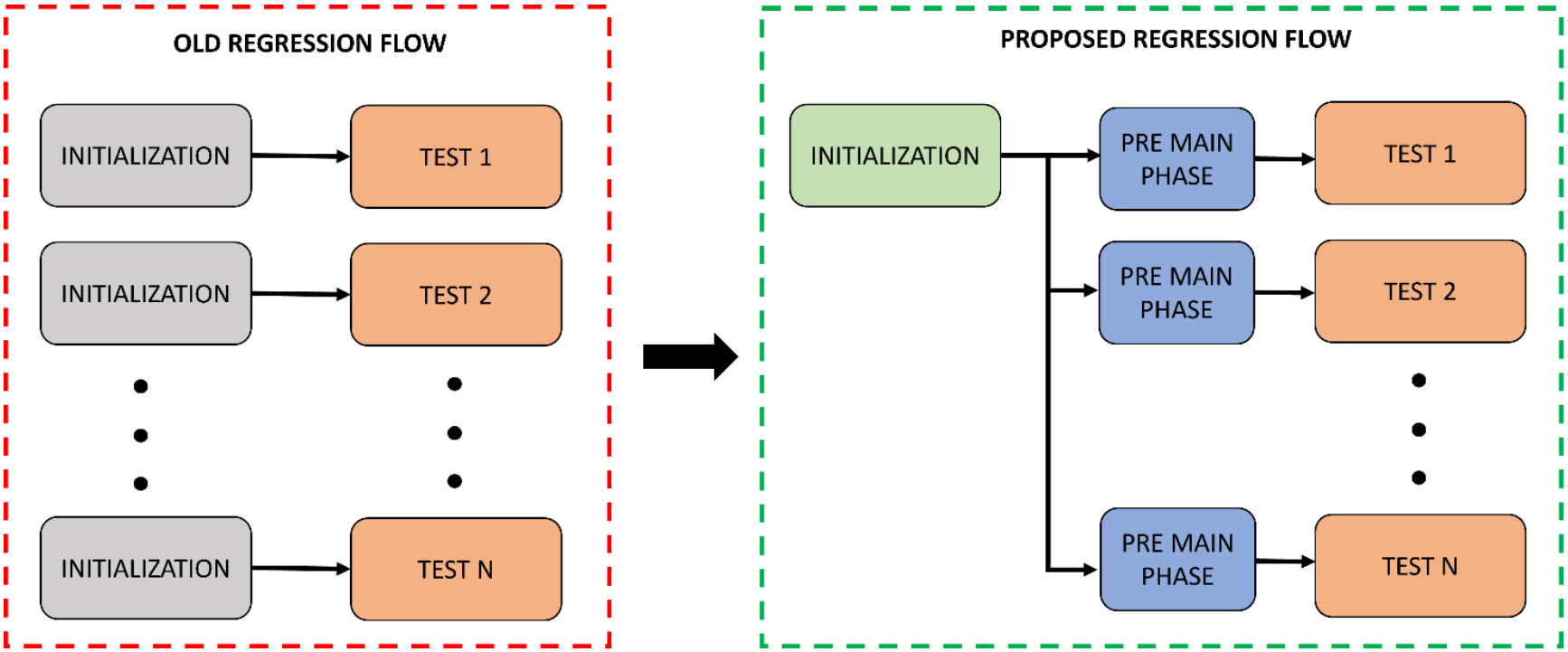


Compliant standard UVM

Reduced simulation time

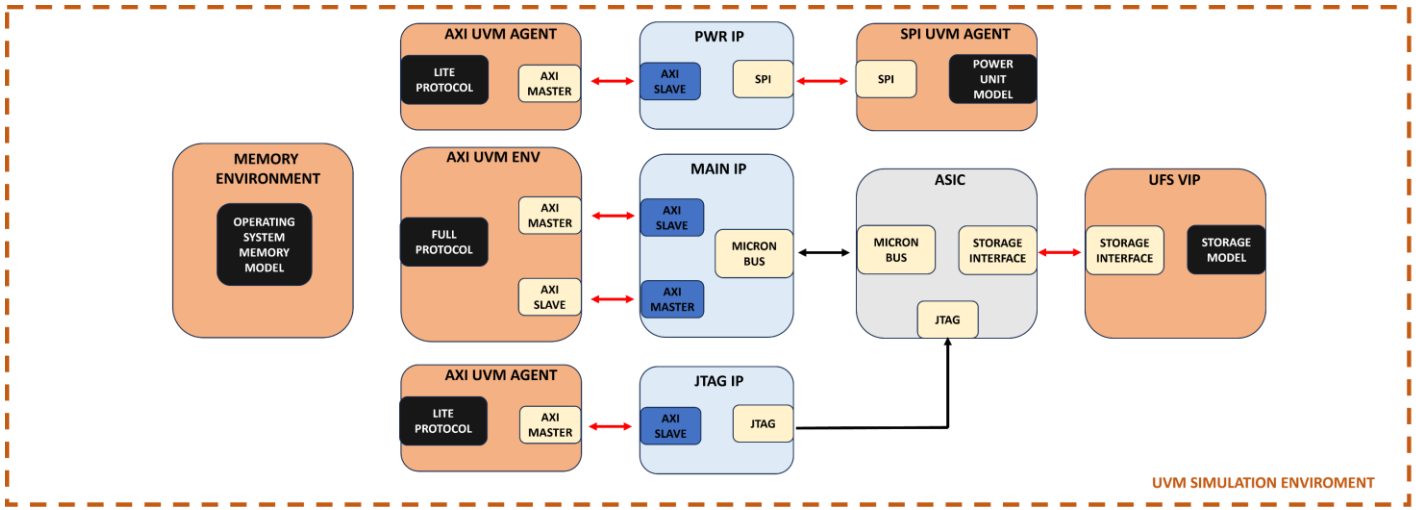
PhD Thesis: validation and debug

- A novel **save and restart technique** for Micron System:

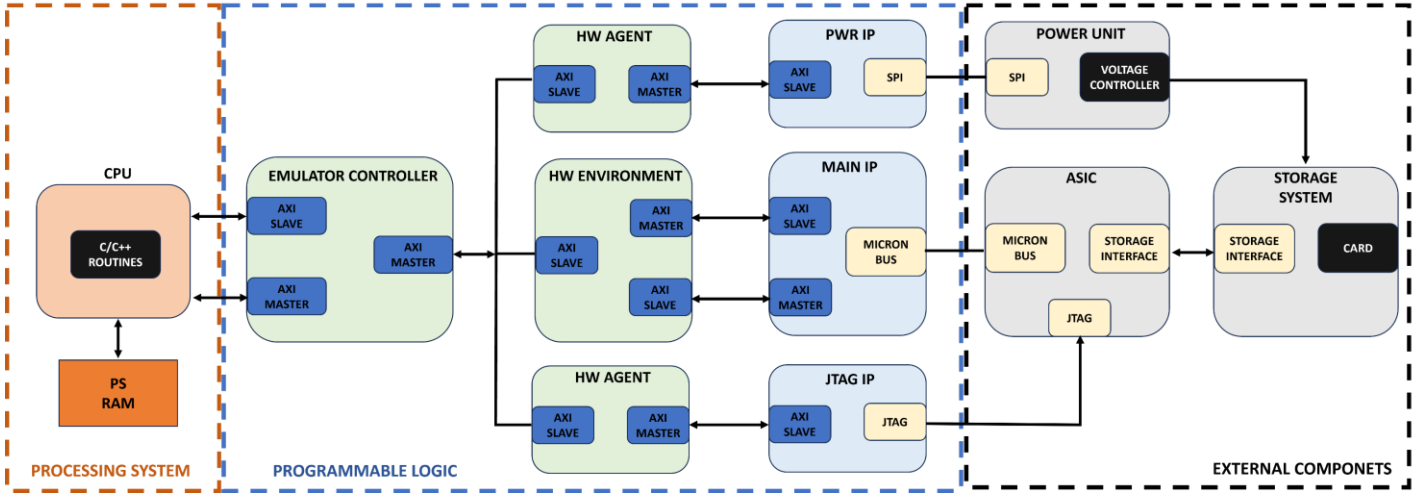


	N° Scenario	N° Test	Regression Time	% Simulation Time Saved	% Test Reduced
Micron	82	82	**14 h 39 m**	-	-
Proposed	82	58	**11 h 48 m**	**19.5**	**29.3**

PhD Thesis: emulation



Simulation



Emulation

PhD Thesis: emulation

- Motivations:
  - **Target coverage**: reachable by means the evaluation of 20K scenarios.
  - **Estimated simulation time**: 5 minutes for each scenarios.

- Emulation allows achieving both goals.
- Experimental results in Micron Technology to evaluate 20K different scenarios:

	N° Scenarios	Execution Time	Target Coverage
Software approach	20 K	**~ 7 days**	**UNREACHABLE**
Emulation approach	20 K	**~ 5 minutes**	**ACHIEVED**

PhD thesis overview: hardware accelerator for NN

- Main operation: finite impulse response linear computation

$$y(n) = \sum_{i=0}^{k-1} x(n-i)h(i)$$

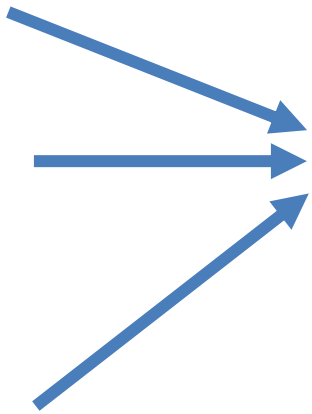
- Hardware implementation: multiply-accumulate (MAC)
- Typical neural network requires a few millions MACs
- Parallel computation and reuse of partial values:

$$y(j) = \sum_{i=0}^{k-1} x(j-i)h(i)$$

$$y(j-1) = \sum_{i=0}^{k-1} x(j-1-i)h(i)$$

$$\vdots$$

$$y(j-k) = \sum_{i=0}^{k-1} x(j-k-i)h(i)$$



Fast Fir Algorithm

Rewritten in order to **share partial values**

PhD thesis: hardware accelerator for NN

- Alphabet chosen for shared partial values:

$$P_{typeI}(\delta,\gamma,i)=\sum_{j_1=\delta}^{\delta+\gamma} x(k\cdot i-1-j_1)\cdot\sum_{j_2=k-(\delta+\gamma)-1}^{k-\delta-1} h(j_2)$$

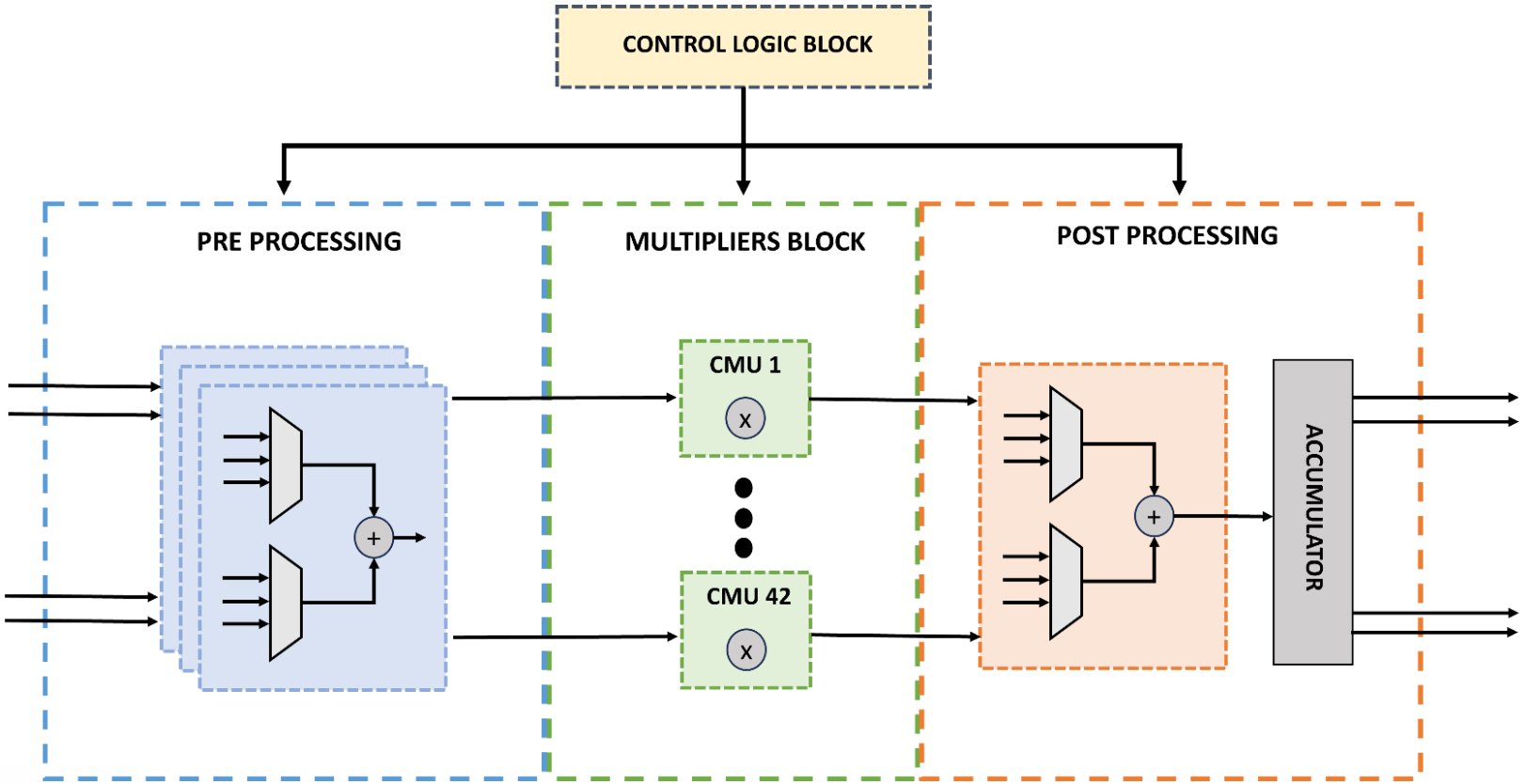
$$P_{typeII}(\delta,\gamma,i)=$$
$$[x(k\cdot i-1-\delta)+x(k\cdot i-1-(\delta+\gamma))]\cdot[h(k-(\delta+\gamma)-1)+h(k-\delta-1)]$$

$$\delta,\gamma\in[0,k-1]$$

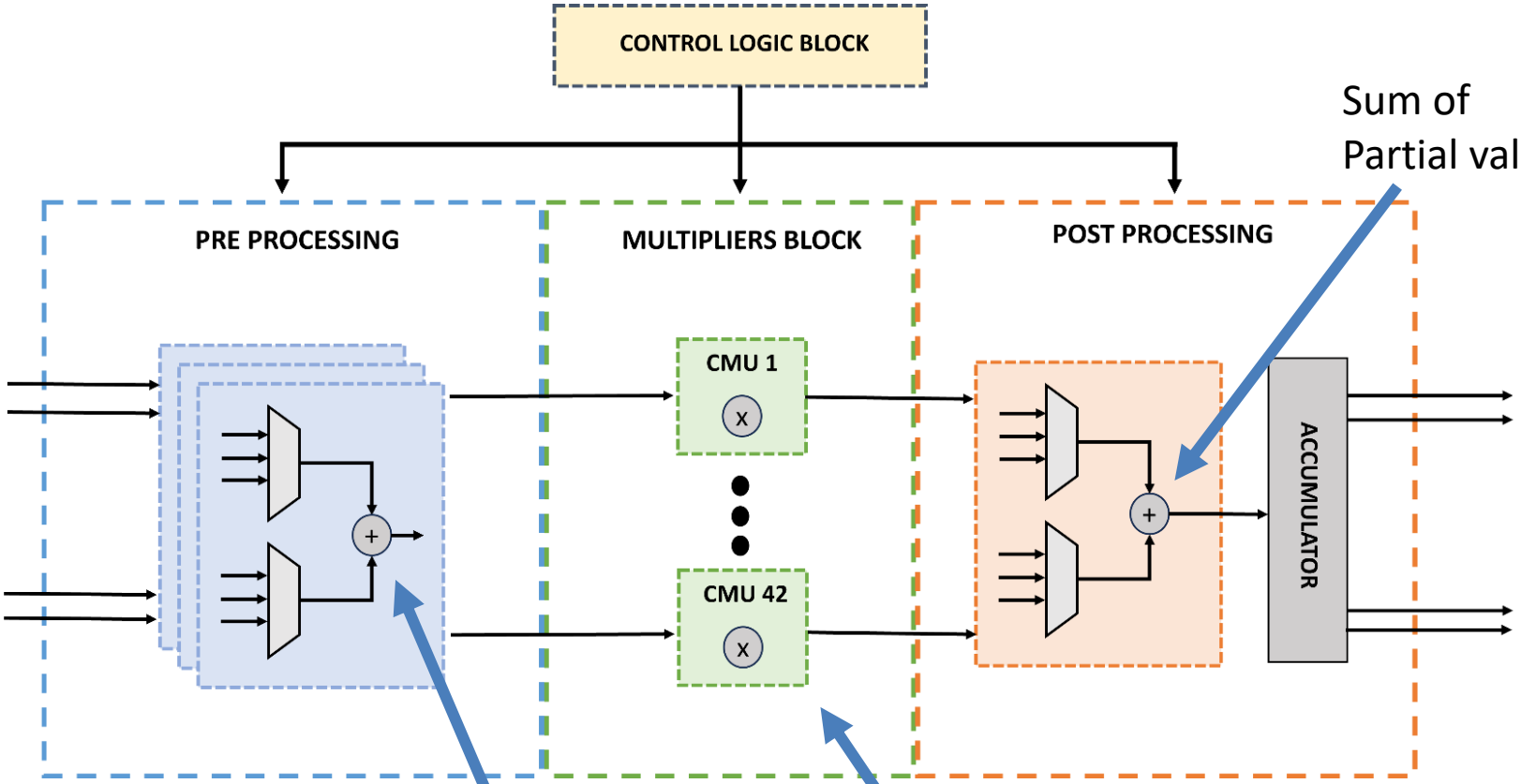
- Each partial value requires 1 multiplication.
- Several possible alphabets: algorithmic search of a reduced size alphabet **for each filter size**.

PhD Thesis: hardware accelerator for NN

- Hardware implementation of the Fast FIR Algorithm applied to **Alex-Net**.
- **Test chip** fabricated in $28\ nm$ TSMC CMOS technology.
- **Reconfigurable hardware accelerator:** same accelerator for different network layers.

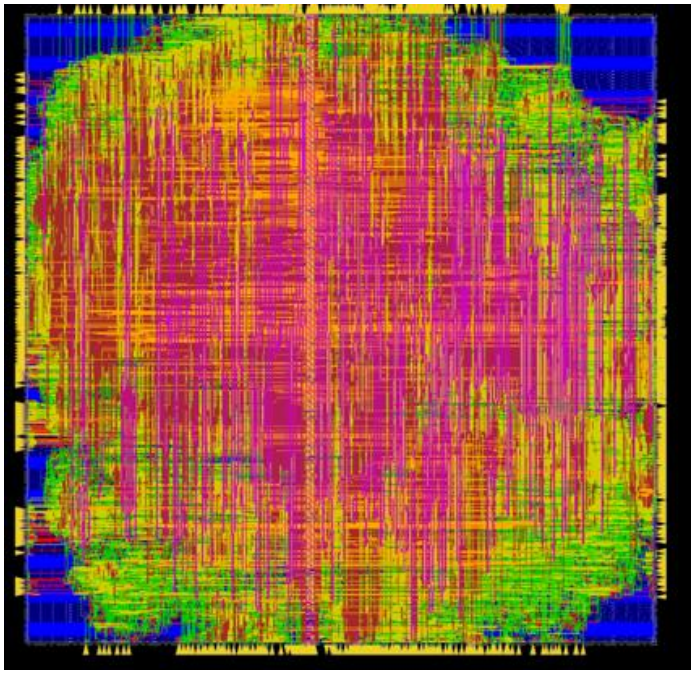


PhD Thesis: hardware accelerator for NN



$$P_{typeI}(\delta,\gamma,i) = \sum_{j_1=\delta}^{\delta+\gamma} x(k\cdot i-1-j_1) \cdot \sum_{j_2=k-(\delta+\gamma)-1}^{k-\delta-1} h(j_2)$$

PhD Thesis- Test chip Layout



Technology	TSMC CMOS $28nm$
Area(mm^2)	0.152
Power dissipation (mW)	68.24
Frequency (MHz)	500

Layer	Kernel	Multiplications required from standard convolution	Multiplications required from proposed algorithm	Proposed Datapath Latency (clock cycles)
1	11x11	105×10^6	76×10^6	0.8×10^6
2	5x5	223×10^6	143×10^6	1.75×10^6
3	3x3	149×10^6	115×10^6	1.35×10^6
4	3x3	112×10^6	86×10^6	1×10^6
5	3x3	74×10^6	57×10^6	0.7×10^6

Thanks for the attention !