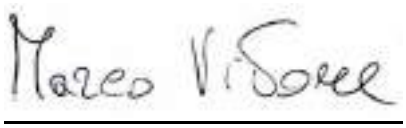
PhD in Information Technology and Electrical Engineering
Università degli Studi di Napoli Federico II

PhD Student: Marco Vitone

Cycle: XXXVI

Training and Research Activities Report

Year: First



Tutor: Prof. Prof. Nicola Petra

Co-Tutor: Ing. Claudio Giaccio (Micron Semiconductor Italia)

Date: October 21, 2021

1. Information:

- **PhD student: Marco Vitone**
- **DR number: DR995147**
- **Date of birth: 11/10/1994**
- **Master Science degree: Electrical Engineering University: Università degli studi di Napoli Federico II**
- **Doctoral Cycle: XXXVI**
- **Scholarship type: *Funded by Micron Semiconductor Italia S.R.L.***
- **Tutor: Prof. Nicola Petra**
- **Co-tutor: Ing. Claudio Giaccio**

2. Study and training activities:

Activity	Type[1]	Hours	Credits	Dates	Organizer	Certificate[2]
Digital Forensics' methods practices and tools	Course	10	3	03-05-06-09-10/11/2020	Dr. G. Cozzolino	Y
Dispositivi e Sistemi Fotovoltaici	M.Sc. Course	72	9		Prof. Santolo Daliento	Y
Data Science for Patient Record Analysis	Course	10	2.5	10-17-24/02 and 03-17/03	Prof. Marcello Cinque	Y
Scientific Programming and Visualization with Python	Course	10	2	08-10/03	Prof. Alessio Botta	Y
Statistical data analysis for science and engineering research	Course	12	4	17-19-24-25/02 and 03-17/03	Prof. Roberto Pietrantuono	Y
Electronics for IoT	PhD School	17	3.4	5-7/7/2021	Associazione Società Italiana di Elettronica	Y
Imprenditorialità Accademica	Course	18	4	7-8-14-15-21-22-23/06/21 and 07-16/07/21	Prof. Pierluigi Rippa	Y
Strategic Orientation for STEM Research & Writing	Course	27	4	15-22/06 8-15-22-29/07	Dr. Chie Shin Fraser	N

				16-23/09 14/10		
Digital Project Management: practices, processes, techniques, tools and scientific approach	Seminar	1	0.2	18/11/2020	Prof. Flora Amato Prof. Giuseppe Longo	Y
#andràtuttobene: Images, Texts, Emojis & Geodata in a Sentiment Analysis Pipeline	Seminar	1.5	0.3	25/11/2020	Prof. Flora Amato Prof. Giuseppe Longo	Y
At the Nexus of Big Data, Machine Intelligence, and Human Cognition	Seminar	1	0.2	2/12/2020	Prof. Flora Amato Prof. Giuseppe Longo	Y
Exploiting Deep Learning and Probabilistic Modeling for Behavior Analytics	Seminar	1	0.2	9/12/2020	Prof. Flora Amato Prof. Giuseppe Longo	Y
Data Driven Transformation in WINDTRE through Managers voice	Seminar	2	0.4	16/12/2020	Prof. Flora Amato Prof. Giuseppe Longo	Y
From Photometric Redshifts to Improved Weather Forecast an interdisciplinary view on machine learning	Seminar	1	0.2	13/1/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
Cybercrime and electronic evidence, The international legal framework for an effective criminal justice response	Seminar	1	0.2	20/1/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
Artificial Intelligence for notary's sector - a case study	Seminar	1	0.2	21/1/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
Machine Learning:	Seminar	1.5	0.3	10/2/2021	Prof. Flora	Y

causality lost in translation					Amato Prof. Giuseppe Longo	
Approaches to Graph Machine Learning	Seminar	1	0.2	17/2/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
Visual Interaction and Communication in Data Science	Seminar	2	0.4	3/3/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
Big Data and Computational Linguistics	Seminar	2	0.4	10/3/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
Sensoria Health	Seminar	1	0.2	17/3/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
DoveAndiamoDomani - Deep Tech	Seminar	1.5	0.3	28/3/2021	Prof. Flora Amato Prof. Giuseppe Longo	Y
Robot Manipulation and Control	Seminar	2.5	0.5	17/11/2020	Prof. Bruno Siciliano	Y
Patent Searching Best Practices with IEE Xplore	Seminar	1	0.2	27/11/2020	IEEE	Y
How to Get Published with IEEE	Seminar	1.5	0.3	2/12/2020	IEEE	Y
Network System, Kuramoto Oscillators and Synchronous Power Flow	Seminar	1.5	0.3	3/12/2020	Scuola Superiore Meridionale	Y
Measuring the Expansion of the Universe with Quasars	Seminar	1.5	0.3	10/12/2020	Scuola Superiore Meridionale	Y
GDPR basics for computer scientists.	Seminar	1.5	0.3	10/12/2020	Prof. P. Bonatti	Y

Synchronization: A Universal Concept in Non Linear Science	**Seminar**	**1.5**	**0.3**	**14/1/2021**	**Scuola Superiore Meridionale**	**Y**
Probing gravitational field: A fundamental viewpoint	**Seminar**	**1.5**	**0.3**	**21/1/2021**	**Scuola Superiore Meridionale**	**Y**
Quantum Simulators	**Seminar**	**1.5**	**0.3**	**28/1/2021**	**Scuola Superiore Meridionale**	**Y**
Engineering the firearm ecosystem: research on media coverage and firearm acquisition in the aftermath of a mass shooting	**Seminar**	**1.5**	**0.3**	**4/2/2021**	**Scuola Superiore Meridionale**	**Y**
Measuring the cosmological parameter with SNe-la and Gamma-ray Bursts	**Seminar**	**1.5**	**0.3**	**11/2/2021**	**Scuola Superiore Meridionale**	**Y**
The SHiP project at Cern	**Seminar**	**1**	**0.2**	**25/2/2021**	**Scuola Superiore Meridionale**	**Y**
Astroparticle Physics in the era of Multi-messenger Astronomy	**Seminar**	**1.5**	**0.3**	**4/3/2021**	**Scuola Superiore Meridionale**	**Y**
Hierarchical Seismic Imaging	**Seminar**	**1.5**	**0.3**	**11/3/2021**	**Scuola Superiore Meridionale**	**Y**
Additive Manufacturing. A world full of opportunities and challenges!	**Seminar**	**1.5**	**0.3**	**18/3/2021**	**Scuola Superiore Meridionale**	**Y**
The coming revolution of Data driven Discovery (a fourth Methodological Paradigm of Science)	**Seminar**	**1.5**	**0.3**	**25/3/2021**	**Scuola Superiore Meridionale**	**Y**
Why Do We Cooperate? Understanding and Modelling Societies using Reinforcement Learning	**Seminar**	**1.5**	**0.3**	**1/4/2021**	**Scuola Superiore Meridionale**	**Y**

Rheo-Engineering Microfluidics: How to exploit the rheological properties of fluids to design microfluidic applications	**Seminar**	**1.5**	**0.3**	**8/4/2021**	**Scuola Superiore Meridionale**	**Y**
Classical Cepheids as distance indicators: from the Milky Way to the Hubble constant	**Seminar**	**1**	**0.2**	**15/4/2021**	**Scuola Superiore Meridionale**	**Y**
Microgravity Science and Technology: an overview	**Seminar**	**1**	**0.2**	**22/4/2021**	**Scuola Superiore Meridionale**	**Y**
Putting more PHYS into PSHA: Advancing Seismic Hazard Analysis with Physics-Based Modelling	**Seminar**	**1.5**	**0.3**	**29/4/2021**	**Scuola Superiore Meridionale**	**Y**
Modelling the Complexity of Multiagent Activity for Human-AI Interaction using Dynamical Primitives	**Seminar**	**1.5**	**0.3**	**6/5/2021**	**Scuola Superiore Meridionale**	**Y**
Dynamics of PDEs and recurrent motions	**Seminar**	**1.5**	**0.3**	**3/6/2021**	**Scuola Superiore Meridionale**	**Y**

1) Courses, Seminar, Doctoral School, Research, Tutorship
2) Choose: Y or N

2.1. Study and training activities - credits earned

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	**3**	**3.2**	**4**	**0**	**10.2**
Bimonth 2	**9**	**3**	**2**	**0**	**14**
Bimonth 3	**8.5**	**3.9**	**2**	**0**	**14.4**
Bimonth 4	**0**	**0.6**	**8**	**0**	**8.6**
Bimonth 5	**7.4**	**0**	**1.6**	**0**	**9**
Bimonth 6	**4**	**0**	**6**	**0**	**10**
Total	**31.9**	**10.7**	**23.6**	**0**	**66.2**
Expected	**30 - 70**	**10 - 30**	**80 - 140**	**0 – 4.8**	

3. Research activity:

System on Chip is a complex Integrated Circuits that includes several components as CPU, Programmable Logic (FPGA), on-chip memory, storage interfaces and so on.
The design of SoC foresees many aspects to be solved, form the implementation of the hardware accelerator to the validation and debug of the SoC architecture. Increasing the complexity of SoC, the design of the letter becomes challenging.
My research activity focuses on design of System on Chip, dealing with both hardware implementation and validation of SoC.
For the sake of clarity, I divided my research activity report into two sub-section:

1. Development of hardware accelerator for SoC
2. Development of methodologies for validation and debug of SoC

1- Development of hardware accelerator for SoC

During last decades, we are witnessing an ever-increasing growth of Neural Network and Machine Learning application. During my first year of PhD course, I analyzed the Convolutional Neural Networks (CNN)[1-3], a specific group of neural networks, that are often implemented by means of hardware acceleration on System on Chip Devices. CNN are characterized by a huge number of layers; each layer computes several bi-dimensional convolutions between the input of the layer and constant kernels. The convolutions require the computation of a large number of multiplications and additions; therefore, I proposed a reconfigurable data-path that allows the hardware acceleration of the computations performed in a CNN.

The SoC proposed is based on a novel k-parallel fast finite impulse response algorithm (FFA) [2],[3] that allows computing k elements of the convolutions result in parallel with reduced number of multiplications; thus, the required hardware resources are drastically reduced.

2-Development of methodologies for validation and debug of SoC

The validation and debug of SoC requires a great effort and time consumption due to the complexity of these architectures. Thereby, a systematic and methodological approach is needed to address this issue.

Accellera Systems Initiative developed the Universal Verification Methodology (UVM) [4] which was accepted by IEEE as a standard. The UVM is a methodology for the functional verification of digital hardware; thus, this methodology allows developing of reusable and robust simulation environment for SoC validation purposes.

My research activity focuses on development of simulation environment for SoC adopting UVM techniques. Over the last year, I collaborated Micron Hardware Validation Tool Team to implement a UVM-based simulation environment for a custom Micron SoC (All rights are reserved). The SoC architecture includes several hardware accelerators, bus interfaces (AXI bus, JTAG bus), and storage interfaces (Universal Flash Storage). By using the UVM approach, the simulation environment is improved in terms of reusability, robustness and coverage analysis. The proposed environment for the SoC validation achieves high speed performance thus reducing the simulation time compared to previous no-UVM simulation environment, developed by Micron.

First achievement: my proposal allows to speed up the performance of the simulation for the 50% regarding to previous proposal.

References

[1] Chao Cheng, Keshab K. Parhi ,"*Hardware efficient fast parallel FIR filter structures based on iterated short convolution*"**,** IEEE Transactions on Circuits and Systems I: Regular Papers**,** 2004.

[2] J. Wang et al., "*Efficient Hardware Architectures for Deep Convolutional Neural Network*", IEEE Transactions on Circuits And Systems–I: Regular Papers, vol.65, n. 6, 2018, pp. 1941-1953.

[3] Yue-Jin Lin, Tian Sheuan Chang, "*Data and Hardware Efficient Design for Convolutional Neural Network*"**,** IEEE Transactions on Circuits and Systems I: Regular Papers, 2018

[4]Accellera(2012),"*Universal Verification Methodology (UVM) 1.1 User 's Guide*",[Online], Aviable : https://www.accellera.org/downloads/standards/uvm

4. Research products:

Vitone, M.; Petra,N.
"Reconfigurable Datapath for Hardware Acceleration of Convolutional Neural Network"
SIE-2021, 52nd Annual Meeting of Associazione Società Italiana di Elettronica

5. Conferences and seminars attended

- *SIE-2021*, *52nd Annual Meeting of Associazione Società Italiana di Elettronica*, on-line conference, 7-9 July 2021.

6. Activity abroad:

7. Tutorship

Cycle: XXXVI **Author: Marco Vitone**