Gerardo Saggese

Autonomous In-vivo Brain-Machine-Interface in 28nm-CMOS technology with Ultrasound-based Power-Harvester and Communication-Link (Brain28nm)

Tutor: prof. Antonio G.M. Strollo

Cycle: XXXVI

Year:2020/2021

My background

Double MSc degree in **Electronic Engineering** and in **Electronics and Telecommunications** – Jan/Feb 2020

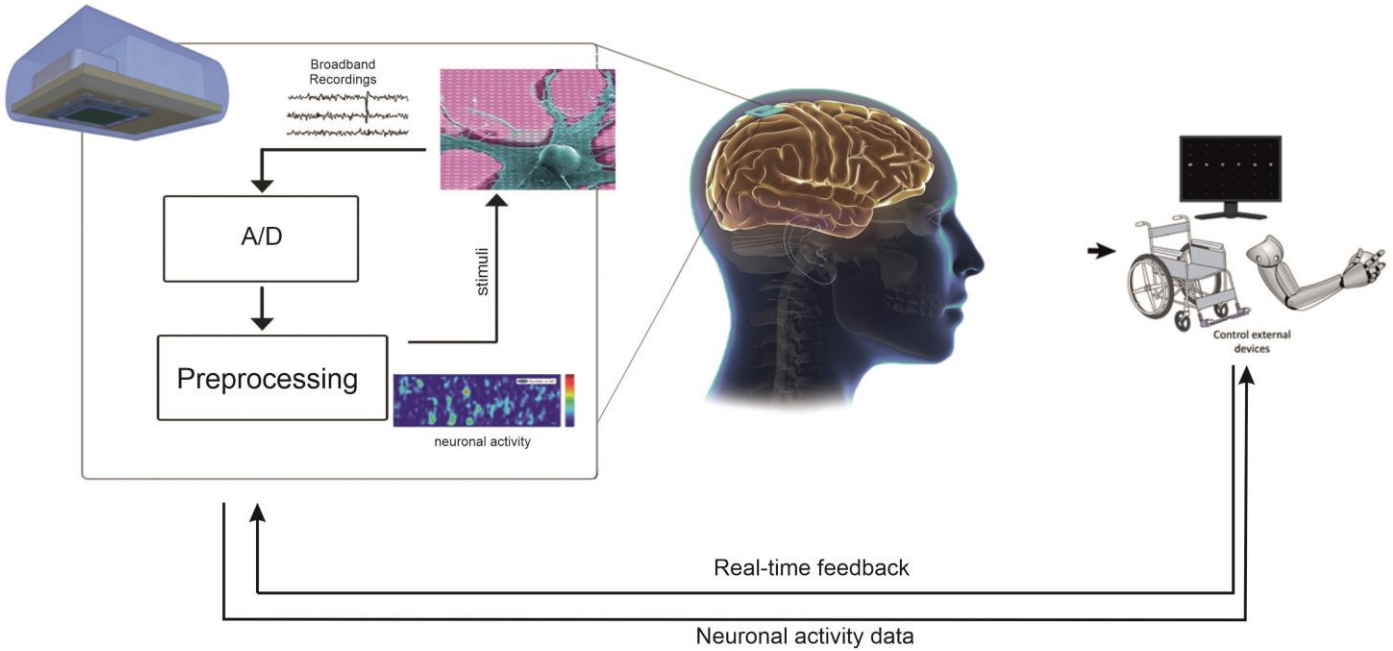
Ph.D. started in November 2020 (XXXVI cycle)

Tutor: prof. **Antonio G.M. Strollo**

My Ph.D. scholarship is founded by **MIUR – PRIN 2017**

Research field of interest

Study, analysis and implementation of **spike detectors** for multichannel **B**rain **M**achine **I**nterface.



Research activity: Overview

Problem:

High density of microelectrodes on a single chip allows the monitoring of a wide neurons' population. This, however, sets a major challenge for a **limited power budget** of an **implantable** device.

Objective:

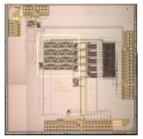
The communication bandwidth and power **constraints** claim for an **on-fly** data reduction block. The **spike detector** is one way of accomplishing it.

Intended contribution:

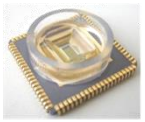
To provide the most suitable spike detector which offers the best **trade-off** between detection performance and computational efforts/power consumptions.

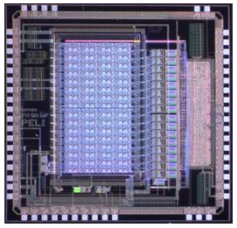
Technology

Multi
Electrode
Array

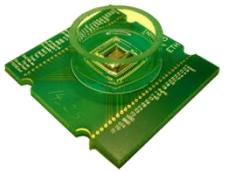


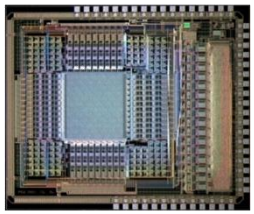
- 16 electrodes
- 16 channels



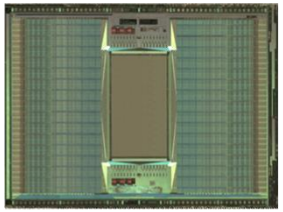


- 128 electrodes
- 128 channels



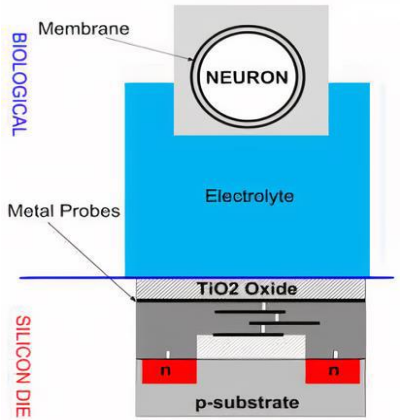


- 11k electrodes
- 126 channels



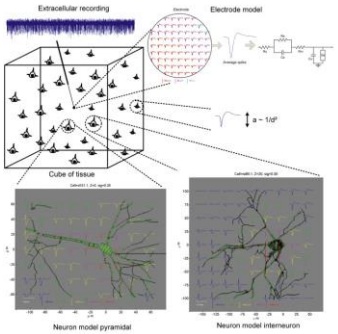
- 26k electrodes
- 1024 channels

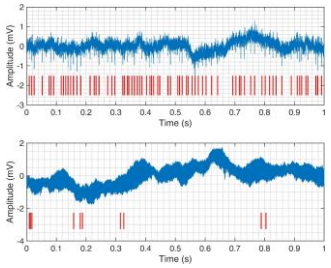
Electrolyte
Oxide
Metal
Oxide
Semiconductor



Methodologies

Synthetic Dataset with known ground truth

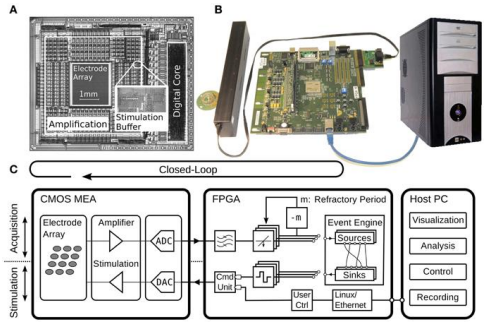




Real extracellular recording with annotated ground truth

MATLAB

Closed-**l**oop approach **FPGA** design and integration with **MEAs** and analogue front-end

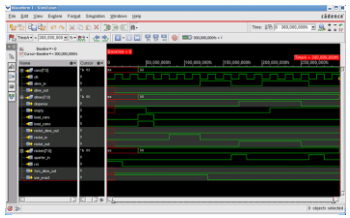


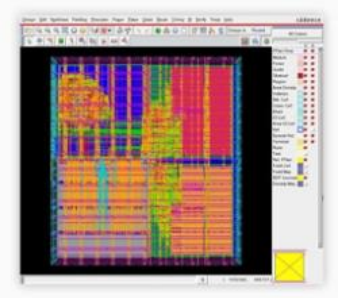
VIVADO™

QUARTUS™

ASIC design and implementation with 28 nm CMOS Technology

cadence





Products

Journal contributions

[1-j]	M. Tambaro., E.A Vallicelli, **G. Saggese**, A.G.M Strollo, A. Baschirotto, S. Vassanelli "Evaluation of In Vivo Spike Detection Algorithms for Implantable MTA Brain—Silicon Interfaces." in *Journal of Low Power Electronics and Applications*. 2020; 10(3):26.
[2-j]	G. D. Meo, D. De Caro, **G. Saggese**, E. Napoli, N. Petra and A. G. M. Strollo, "A Novel Module-Sign Low-Power Implementation for the DLMS Adaptive Filter With Low Steady-State Error." in *IEEE Transactions on Circuits and Systems I: Regular Papers*.
[3-j]	**G. Saggese**, M. Tambaro, E.A Vallicelli, A.G.M Strollo, S. Vassanelli, A. Baschirotto, M.D Matteis," Comparison of Sneo-Based Neural Spike Detection Algorithms for Implantable Multi-Transistor Array Biosensors." in *Electronics* 2021,*10(4)*:410.
[4-j]	**G. Saggese**, A.G.M Strollo, "Low-Power energy-based spike detector ASIC for implantable multichannel BMI" in Journal of Neuroscience method (**submitted**)
[5-j]	**G.Saggese**, A.G.M Strollo "A 1024-channels spike detector RAM latch-based for real-time Brain - Silicon Interfaces", in *Electronics (**in preparation**).*

Conference contributions

[1-c]	M. Tambaro, E. A Vallicelli, **G. Saggese** , A. La Gala, M. Maschietto, A. G. M Strollo, M. De Matteis, A. Baschirotto, S. Vassanelli "A scalable spike detection method for implantable high-density multielectrode array," *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*, 2021, pp. 1-4.

Summary of activities

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	0	3.2	3.5	0	6.7
Bimonth 2	9	3.6	5	0	17.6
Bimonth 3	6	3	5	0	14
Bimonth 4	15	3.9	4	0	22.9
Bimonth 5	0	0	3	0	3
Bimonth 6	0	0	6	0	6
Total	30	13.7	26.5	0	70.2
Expected	30 - 70	10 -30	80 -140	0 – 4.8	

Ad hoc courses

- Scientific Programming and Visualization with Python, 8-10/03/2021
- Statistical data analysis for science and engineering research, 17/02-3/04/2021

MSc and BSc courses

- Circuiti per DSP, 18/09-23/12/2020
- Sistemi Elettronici Programmabili, 30/03-7/06/2021
- Cambridge First Certificate English, 3/03-1/06/2021

Workshops

- ❑ “Introduction to FPGAs and the Intel Quartus Prime Software”, 24/5/2021.
- ❑ “Introduction to Simulation and Debug of FPGAs”, 7/06/2021

Thank you for your kind attention