UNIVERSITÀ DEGLI STUDI DI NAPOLI
FEDERICO II

itee PhD
information technology
electrical engineering

DIETI. UNINA

Gerardo Saggese

Autonomous In-vivo Brain-Machine-Interface in 28nm-CMOS technology with Ultrasound-based Power-Harvester and Communication-Link (Brain28nm)

Tutor: prof. Antonio G.M. Strollo

Cycle: XXXVI

Year:2021/2022

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information technology
electrical engineering

My background

Double MSc degree in **Electronic Engineering** and in **Electronics and Telecommunications** – Jan/Feb 2020

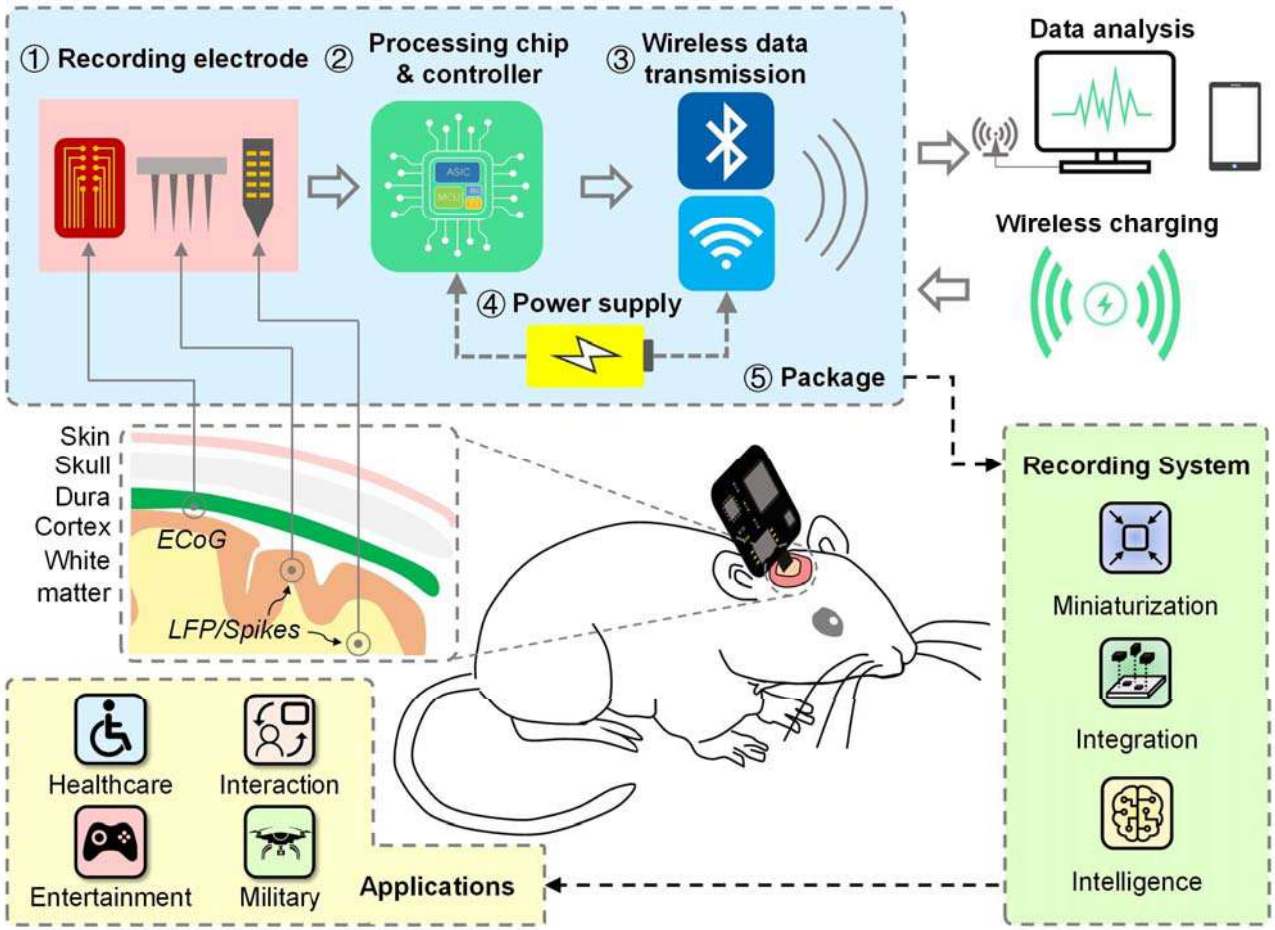
Ph.D. started in November 2020 (XXXVI cycle)

Tutor: prof. **Antonio G.M. Strollo**

My Ph.D. scholarship is founded by **MIUR – PRIN 2017**

Research field of interest

Study, analysis and implementation of **spike detectors** for multichannel **B**rain **M**achine **I**nterface.



Research activity: Overview

Problem:

Nowadays, neural information can be recorded by thousands of electrodes on a single chip, providing an insight of brain activity. However, the increase in the channels count also set a major challenge for the design of a long-term implantable BMIs which rely on a limited power budget and narrow transmission bandwidth.

Objective:

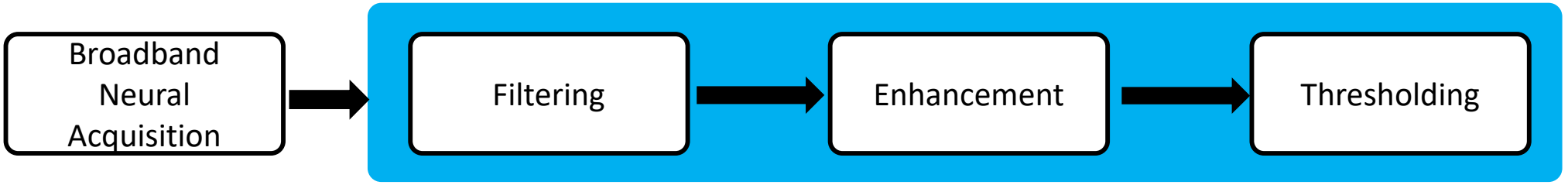
Increased channel count grows the data bandwidth and make it impossible to stream the raw data wireless to MCUs.
This calls for on-implant data reduction pre-processing: **SPIKE DETECTOR.**

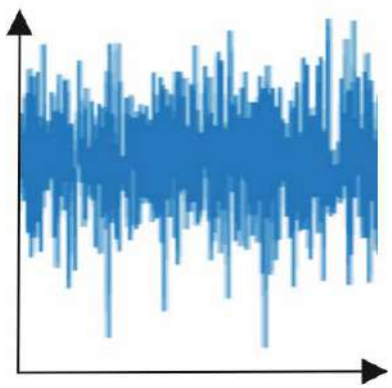
Intended contribution:

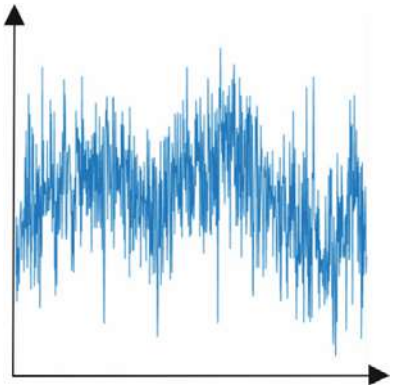
To provide the most suitable spike detector which offers the best **trade-off** between detection performance and computational efforts/power consumptions.

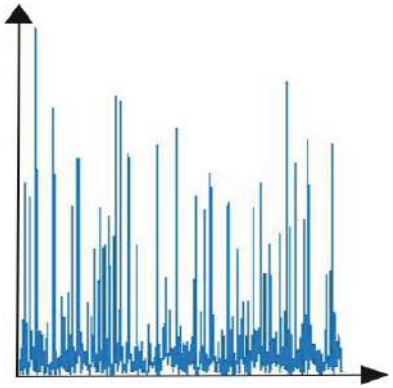
Research activity: Overview

SPIKE DETECTOR WORKFLOW

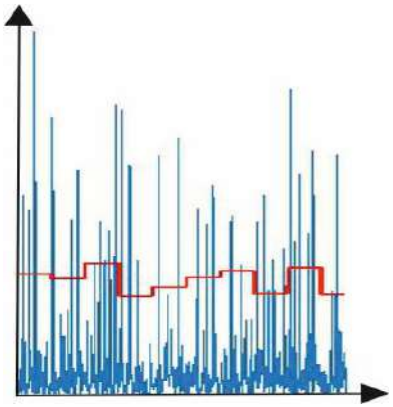








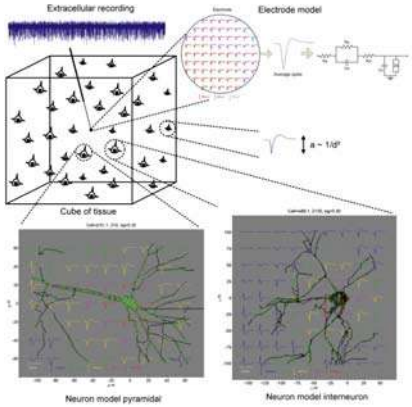
- Template Matching
- Wavelet Transform
- **Energy Operators**
- ML/DL

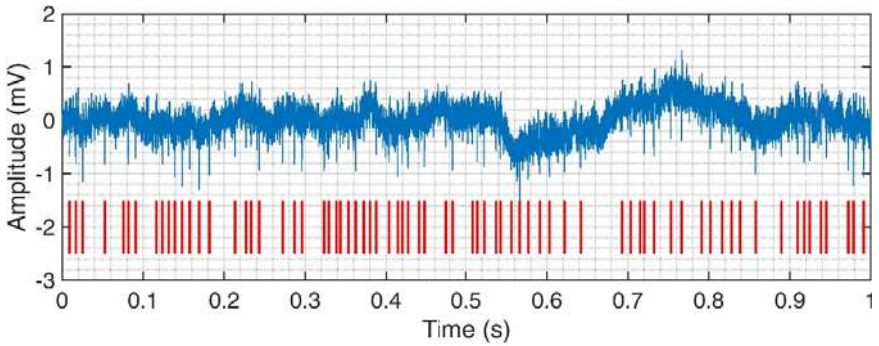


- RMS
- MEAN
- MEDIAN
- **Hybrid**

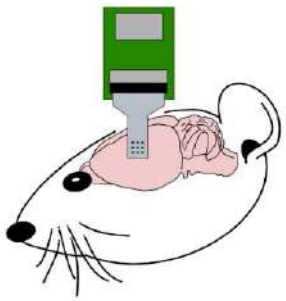
Methodologies

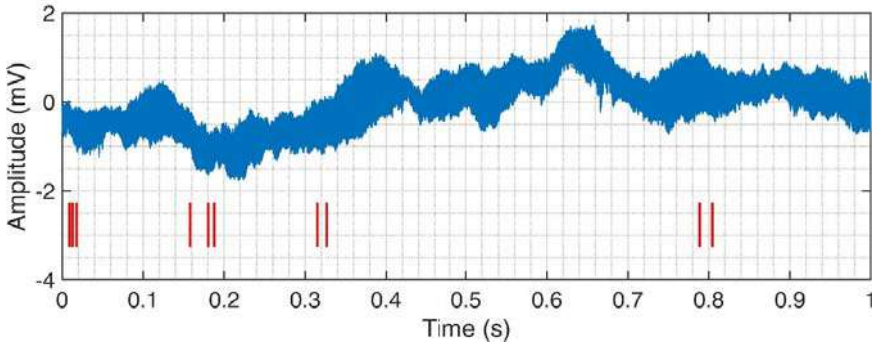
Synthetic Dataset with known ground truth





Real extracellular recording with annotated ground truth

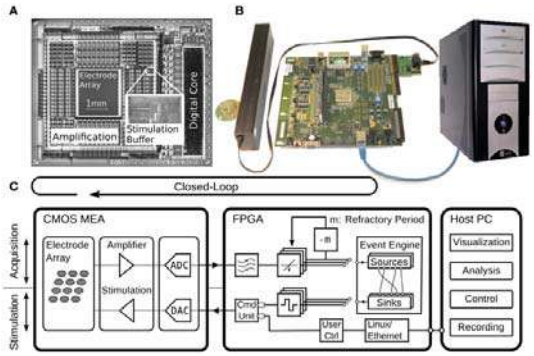




Detection metrics (**Accuracy, Sensibility and Specificity**) depends on many factors (e.g., mechanical/electrical properties as well as biological environmental). Hence, a careful analysis must be carried out to extract the combination of the design parameters which provides satisfactory detection performance.

Methodologies

Closed-**l**oop approach **FPGA** design and integration with **MEAs** and analogue front-end



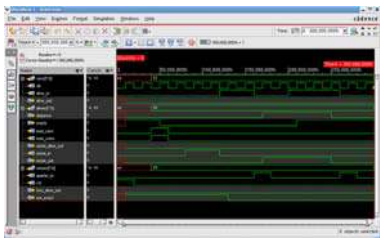
VIVADO™

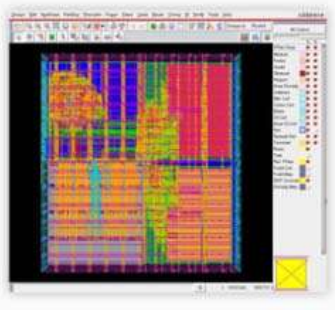
QUARTUS™

A 256-ch SoC spike detectors with programmable filters and threshold section was designed together an AFE interface and TCP/IP communication method to transfer and receive command from/to a host pc. (Ready for the FIELD TEST)

ASIC design and implementation with 28 nm CMOS Technology

cadence





Study and analysis of several low-power techniques aim at reducing the electrical performances of the spike detectors under studied: clock gating, RAM based on Latches, resource sharing etc...

Products

Journal contributions

[1-j]	**G. Saggese** and A. G. M. Strollo, “A Low Power 1024-Channels Spike Detector Using Latch-Based RAM for Real-Time Brain Silicon Interfaces,” Electronics, vol. 10, no. 24, p. 3068, Dec. 2021, doi: 10.3390/electronics10243068.
[2-j]	A. G. M. Strollo, E. Napoli, D. De Caro, N. Petra, **G. Saggese** and G. Di Meo, "Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 6, pp. 2449-2462, June 2022, doi: 10.1109/TCSI.2022.3152921,
[3-j]	E. Zacharelos, I. Nunziata, **G. Saggese**, A. G. M. Strollo and E. Napoli, "Approximate Recursive Multipliers Using Low Power Building Blocks," in IEEE Transactions on Emerging Topics in Computing, vol. 10, no. 3, pp. 1315-1330, 1 July-Sept. 2022, doi: 10.1109/TETC.2022.3186240.
[4-j]	G. Di Meo, **G. Saggese**, A. G. M. Strollo, D. De Caro, and N. Petra, “Approximate Floating-Point Multiplier based on Static Segmentation,” Electronics, vol. 11, no. 19, p. 3005, Sep. 2022, doi: 10.3390/electronics11193005.
[5-j]	**G. Saggese** and A. G. M. Strollo, “Low-Power Energy-Based Spike Detector ASIC for Implantable Multichannel BMIs,” Electronics, vol. 11, no. 18, p. 2943, Sep. 2022, doi: 10.3390/electronics11182943.
[6-j]	G. Di Meo, **G. Saggese**, A. G. M. Strollo and D. De Caro, “ MAC unit using Static Segmentation”, **submitted** to IEEE Transactions on Emerging Topics in Computing.
[7-j]	I. Nunziata, E. Zacharelos**, G. Saggese**, A. M. G. Strollo and E. Napoli, " Approximate Squaring circuits exploiting Recursive Architectures” **submitted** to Integration Elsevier Journal.

Conference contributions

[1-c]	I. Nunziata, E. Zacharelos, **G. Saggese**, A. M. G. Strollo and E. Napoli, "Approximate Recursive Multipliers Using Carry Truncation and Error Compensation," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2022, pp. 137-140, doi: 10.1109/PRIME55000.2022.9816787**.(Golden Leaf award)**
[2-c]	**G. Saggese**, E. Zacharelos and A. G. M. Strollo, "Low Power Spike Detector for Brain-Silicon Interface using Differential Amplitude Slope Operator," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2022, pp. 301-304, doi: 10.1109/PRIME55000.2022.9816758. (**paper presented**)
[3-c]	**G. Saggese** and A.G.M Strollo, "Low-Power Energy-Based Spike Detector for Brain-Silicon Interface" 53rd Annual Meeting of the Associazione Società Italiana di Elettronica (SIE), Pizzo (VV), Italy, 7-9 September 2022 (**poster presented**).

Summary of activities

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	0	4.4	6.5	0	10.9
Bimonth 2	0	0.6	6.5	0	7.1
Bimonth 3	0	1.5	6.5	0	8
Bimonth 4	13	0.6	6	0	19.6
Bimonth 5	8	0	5	0	13
Bimonth 6	4	7	6	0	17
Total	25	14.1	36.5	0	75.6
Expected	30 - 70	10 - 30	80 - 140	0 – 4.8	

Ad hoc/PhD courses & schools

- Ultra-low power integrated systems for green growth to the trillion scale, PhD. Course of Univ. of Pisa. 20/06/22-22/06/22
- Impreditorialità Accademica, 26/05/2022-26/07/22
- Biosignals measurement and analysis, 15/06/22-13/07/22
- Ph.D School “Automotive Electronics“ (SIE22) 05/09/22-07/09/22

MSc and BSc courses

- FPGA per l’elaborazione dei segnali, 30/03/2022-07/06/2022

Workshops

- “Comprehensive Digital IC Implementation & Sign-Off”, 03/10/2022-05/10/2022.

Next Year??

Research Abroad:
Fulda University of Applied Science (Germany)
Jan/Feb-June

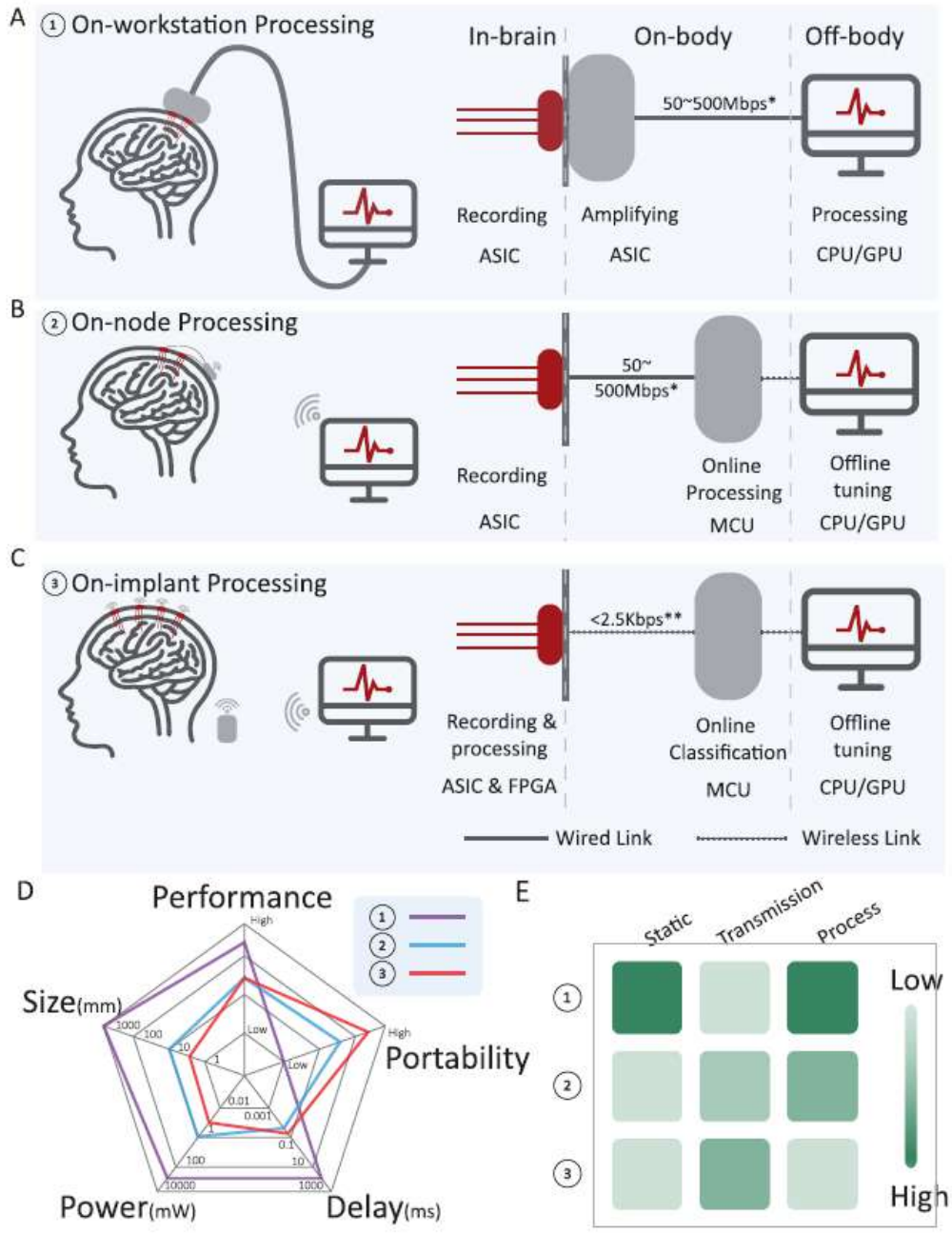
Advanced and Approximate Compressor Tree Synthesis for FPGAs

Prototype 256-ch SoC Spike Detector with AFE interface

- FIELD TEST
- 1024 channels

Approximating Computing and its application in the BMI DSP systems

Thank you for your attention



A: wired BMI systems stream and process the amplified neural activities on the workstation. **B:** wired online signal processing systems stream and process the neural data on MCUs. The model is tuned on a workstation. **C:** distributed wireless online systems pre-process the recording on-implant for bandwidth reduction, reducing the bandwidth of the signal wirelessly sent to the local classifier and response controller (e.g. wearable devices). **D**: a radar diagram for the three systems showing performance, size, power, delay and portability. **E:** a comparison of different types of power consumption for the three BMI systems.

∗ Assuming the sample frequency is 24 414 Hz with 128 to 1024 channels with 16-bit data stream.

∗∗ Assuming the firing rate is 20 Hz with binary data stream, with a total of 128 channels. This data rate can be even reduced with binning and/or compression.