UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

itee PhD information technology electrical engineering

DIETI UNINA

PhD Student
Giuseppe Guida
Embedded Hypervisor security

Tutor: Alessandro Cilardo co-Tutor: …

Cycle: XXXV Year: FIRST

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My background

- MSc degree in Computer Engineering.
- PhD start date 01/11/2019
- No Scholarship
- Currently I am working for Hitachi Rail STS as V&V Signalling Engineer

Research field of interest

- My research field concerns the secure virtualization of embedded devices, especially those equipped with reconfigurable hardware such as FPGAs. By leveraging the concept of Hypervisor and the various security mechanisms available, I am trying to understand how these two aspects are linked together and how to use them efficiently on an FPGA.

Summary of study activities

- As ad hoc PhD courses / schools I attended the following:
  - Software security in the railway context
  - Matlab Fundamentals
  - Virtualization techniques and their applications
  - Enterpreneurship and Start-up
  - Machine Learning
- As Courses attended borrowed from MSc curricula I can list
  - Big Data Analytics
  - Artificial Intelligence
- I attended the PRIN SPHERE 2017 meeting held in Modena on January 22nd, 2020

Research activity: Overview

- Problem

Given an FPGA, is it possible to design a secure hypervisor which manages the reconfiguration without impacting the performance?

Answering this question is important because theoretically using an hypervisor can be achieved more with less hardware.

- Objective
  - Assess the feasibility of secure virtualization by investigating all the security techniques that may fit our purpose and may apply on a particular kind of hypervisor.
- Intended contribution (in perspective)
  - Produce several scientific papers about this matter.
  - Implement (if possible) a working proof-of-concept