ITEE PhD – Ad hoc Course Announcement

Università degli Studi di Napoli Federico II

PhD Programme in Information Technology and Electrical Engineering

Module Title: Safety Critical Systems for Railway Traffic Management

Lecturer: Dr. Mario Barbareschi, PhD

Rete Ferroviaria Italiana, Gruppo Ferrovie dello Stato Italiane
Ricerca e Sviluppo – Sviluppo Sistemi
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CV: Mario Barbareschi received the Ph. D. in Computer and Automation Engineering in 2015 and the Master Degree in Computer Engineering cum laude in 2012, both from the Università degli Studi di Napoli Federico II, Italy, where he worked a post-doctoral fellow until 2019. He is currently employed in Rete Ferroviaria Italiana, member of Gruppo Ferrovie dello Stato Italiane, where he is currently working as senior embedded technology specialist.

Dates and Locations (rooms are in 3A Building, via Claudio 21, Napoli)

Date	Hours	Room
10nd January 2020	9:00-13:00	Sala riunioni IV piano DIETI
13th January 2020	13:00-16:00	Sala riunioni IV piano DIETI
17th January 2020	9.00-13.00	Sala riunioni IV piano DIETI
20nd January 2020	13:00-16:00	Sala riunioni IV piano DIETI
24th January 2020	9:00-12:00	Sala riunioni IV piano DIETI
27th January 2020	13:00-16:00	Sala riunioni IV piano DIETI

ECTS Credits: 3.3

Participants (including those interested to the Tutorship positions, see Notes below) are required to send an e-mail to the lecturer, with the subject "[ITEE] course: Safety Critical Systems for RTM", specifying in the message body their name, master degree title, and a very short description of their research topic.
In addition, participants of the ITEE 36th cycle are required to inform the ITEE Coordinator prior to the course, by sending an email with the same subject as above to: stefano.russo@unina.it.

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Content

I Lesson - Introduction:
The Italian railway system from different points of view: structure of Ferrovie dello Stato and Rete Ferroviaria Italiana. Research and Deploy activities in railway signaling systems, projects and innovation activities.

II Lesson – Computing Architectures:
Fail-safe computing architectures for railway applications: real-time system, 2oo2 architectures, consensus managing, vital and fail-safe output. Model-based approaches for critical software. Laboratory: Matlab Simulink.

III lesson – Security Standards:
Principles of EN 50126, EN 50128 and EN 50129. Software artifacts and V model: SRS, testing plan, design and implementation of critical software. The fundamental role of coding standards for programming languages. MISRA C at a glance and hands-on. Laboratory: Matlab Polyspace.

IV Lesson – Coding a Real-time Operating System - Part 1:
Completion of documentation, software implementation and testing of an RTOS for ARM Cortex M3 Architecture (ARMv7-M). Asynchronous and synchronous interprocess communication. Laboratory: git, continuous integration, cross compilation and debugging, SystemWorkbench for STM32 devices.

V Lesson - Coding a Real-time Operating System - Part 2:
Device driver for external communication, application development: deadline, priority and period of critical tasks. Laboratory: Git, continuous integration, cross compilation and debugging, SystemWorkbench for STM32 devices.

VI Lesson – Model Based Design:
Model based engineering of critical systems. Simulation and testing. From model to software in Matlab Simulink.

Notes

Doctoral Students are requested to bring their own notebook (starting from Lesson II) with SystemWorkbench AC6, Git, Word Processor, Spreadsheet tool, licensed Matlab with Polyspace toolboxes installed. A STM32 development board will be distributed to all attendees.
Doctoral Students with noticeable experience on embedded system, C coding, RTOS and Matlab Simulink can participate as Tutors. In particular, Tutors can be involved as assistants during the last 4 lessons.

Contacts for additional info: **Prof. Antonino MAZZEO** - tel. 081 7683904 – antonino.mazzeo@unina.it
Prof. Nicola MAZZOCCA - tel. 081 7683815 – nicola.mazzocca@unina.it